Key Engineering Materials

Volume - 13

Issue No. 3

September - December 2025

ENRICHED PUBLICATIONS PVT. LTD

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PHONE: - + (91)-(11)-47026006

Key Engineering Materials

Managing Director

Amit Prasad

Key Engineering Materials

(Volume - 13, Issue No. 3, September - December 2025)

Contents

Static Analysis of Temperature-Dependence of Paralleled High VoltageVertical Silicon & SiC NPN BJTs

Chengjun Shen1,a, Saeed Jahdi1,b*, Mana Hosseinzadehlish1,c, Phil Mellor1,d, Konstantinos Floros2,e and Ingo Lüdtke2,
1University of Bristol, Bristol, BS8 1UB, United Kingdom
2Compound Semiconductor Applications Catapult, Newport, NP10 8BE, United Kingdom

ABSTRACT

This paper compares the static properties for Silicon & SiC BJTs when connected in parallel, under various operating temperatures at various base currents and collector currents. This includes analysis of forward I-V characteristics, on-state resistance, DC gain, forward transfer characteristics and reverse leakage current to provide insights on paralleling of SiC & SiC BJTs.

Keywords: Bipolar Junction Transistor, Static Performance, Vertical Devices, Temperature

Introduction

For power applications with voltage requirements lower than 1700 V, SiC BJT can compete with SiC MOSFET because of the absence of gate oxide which could potentially have defects and charge traps [1, 2] as well as its close static and dynamic power dissipation performance [3, 4]. Challenges in fabrication of bipolar power devices are carrier lifetime in conductivity modulation and reverse recovery, bipolar degradation and avalanche ruggedness [5]. Key interests are on static and dynamic performance and electrothermal ruggedness at larger on-state currents and elevated temperatures.

Experimental Set-Up

This paper characterizes the static properties for two-paralleled SiC power BJTs GA04JT17-247 and compare with the similarly rated Silicon BJTs FJL6920 by means of extensive experiments. To conduct experiments, a B2902A Source/Measure Unit (SMU) is directly connected to either power Silicon or SiC BJTs through high-temperature test leads as shown in the Fig. 1. To connect in parallel, two discrete BJTs are directly connected to each other via their leads for minimal parasitic resistance and parasitic inductance. BJTs are placed in a TAS LTCL600 climatic test chamber, as also shown in Fig. 1 to adjust the operating temperature from -50°C to 150°C in steps of 25 degrees.

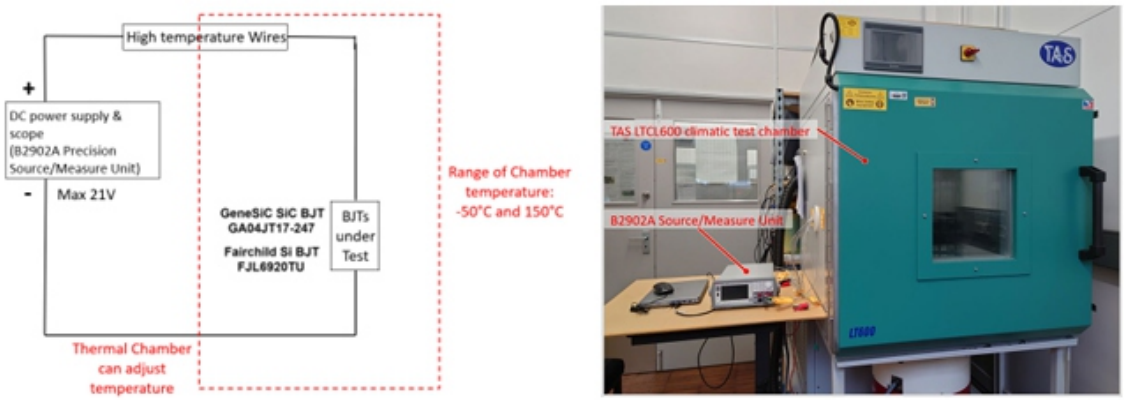

Fig. 1. Schematic and view of the experimental rig for static measurements of power BJTs.

Output Characteristics

To characterize the forward output characteristic, the Collector-Emitter current (ICE) is measured while sweeping the Collector-Emitter voltage (VCE) from 0 to 4 V in 0.04 V increments, with the fixed Base-Emitter current (IBE) of 10 mA, 20 mA and 30 mA used in each set of measurements between -50°C to 150°C. This setting is chosen to ensure the safe operation of both Silicon and SiC BJTs because of the low current rating of SiC BJT at high temperatures while enabling fair comparison between performance of the two devices both in single and paralleled configurations.

In terms of paralleled BJTs, the maximum VCE was set to 1 V from the SMU since the sweeping of VCE cannot continue at higher voltages. Fig. 2 show the output characteristics of the two-paralleled Silicon BJTs under various chamber temperatures. Under such low Collector-Emitter voltages, the increase of collector current with increasing temperature is associated with the increased stored charge in the drift region. This is because with increase of temperature additional carriers will be released intrinsically to contribute to the current conduction while the carrier lifetime also increases [6-8]. The mobility is reduced with temperature, however, the impact of the two aforementioned parameters is more pronounced in increasing the Collector-Emitter current. This in turn leads to increase of the DC gain (β) with temperature in the Silicon BJT.

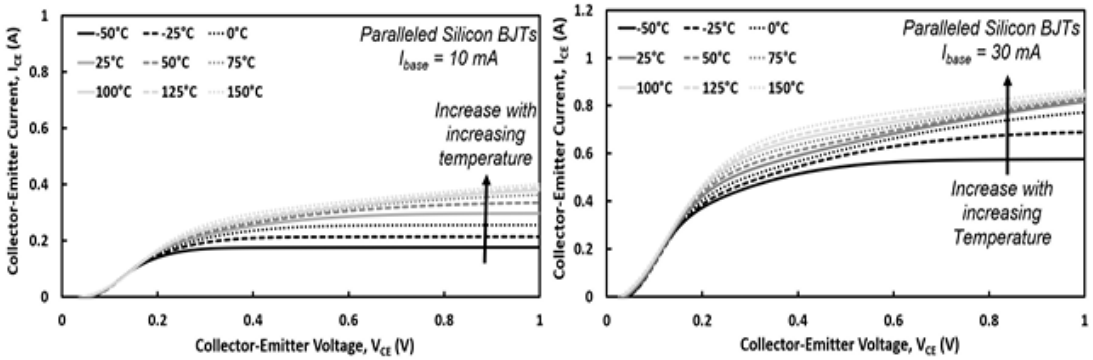

Fig. 2. Forward I-V characteristics for paralleled Silicon BJTs at I_{Base} of 10 mA and 30 mA under different temperatures.

The comparison between the I-V curves of single Silicon BJT and paralleled Silicon BJTs can be found in Fig. 3. When parallel BJTs are conducting a current, the slight difference in device parameters, namely, the on-state resistance of the Base-Emitter region, can cause current mismatch where the low resistivity one carries more base current and thus more collector current. At high base currents, the base current imbalance between paralleled becomes worse. At high chamber temperatures, the higher current device is prone to higher junction temperatures and attracts more current since it is more difficult to extract heat. Both conditions produce a huge difference in collector current between two devices together with a huge difference in Collector-Emitter conduction resistance. Such current imbalance can lead to the smaller on-state resistance of paralleled Silicon BJTs than that of single BJT and thus the larger collector current as can be seen in Fig. 3.

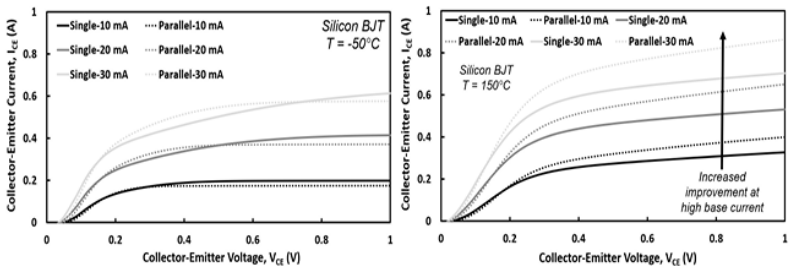

Fig. 3. I-V characteristics for paralleled Silicon BJTs at different base currents at -50°C & +150°C.

For paralleled SiC BJTs as shown in Fig. 4, the decrease of collector current is also observed because of the significant incomplete ionization of acceptors at room temperature in the base region. This in turn leads to the surge of hole concentration at high temperatures and reduces the current gain. The incomplete sweep of Collector-Emitter voltage is due to the current reaches the SMU's limit.

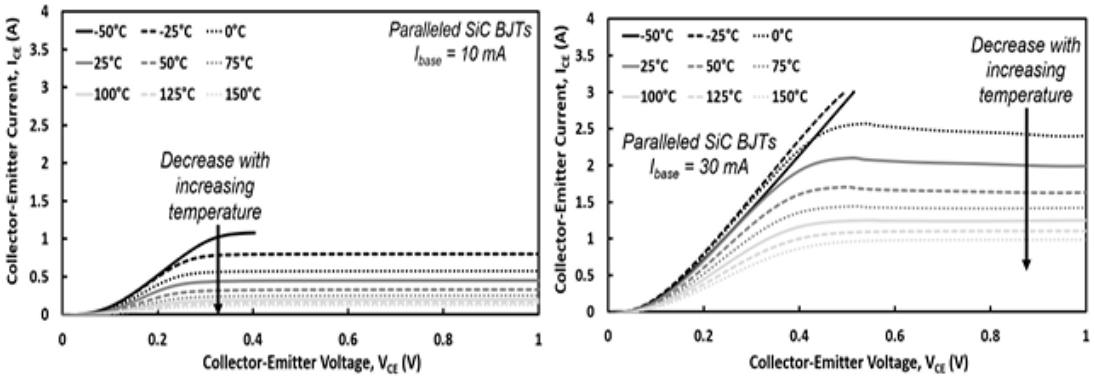

Fig. 4. Forward I-V of parallel SiC BJTs at I_{Base} of 10 mA and 30 mA by temperature.

Unlike the paralleled Silicon BJTs, the current gain in paralleled SiC BJTs reduces compared to its single device, as observed in Fig. 5. This is due to the fact the two devices are sharing the same base current supplied by a single base driver, and at lower base current the Collector-Emitter current drops more than expected due to reduced injection efficiency.

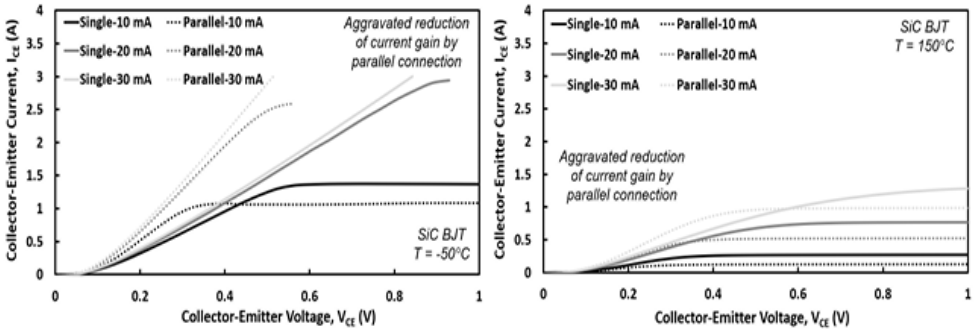

Fig. 5. Comparison of I-V characteristics for the single and paralleled SiC BJTs at different base currents under -50°C and +150°C.

The instability problem of current gain in SiC BJT becomes worse when in parallel connection as the reduction of Emitter efficiency can occur in both SiC devices, where the difference of current gain between paralleled Silicon BJTs and paralleled SiC BJTs is about 28 at 1 V as shown in Fig. 6 while the current gain gap is approximately equal to 20.5 at 4 V. It must be noted that in the case of the paralleled device the base current is supplied by the same base driver and shared between the two paralleled devices, further reducing the base current supplied per device which as expected has led to further reduction of the DC current gain in the SiC.

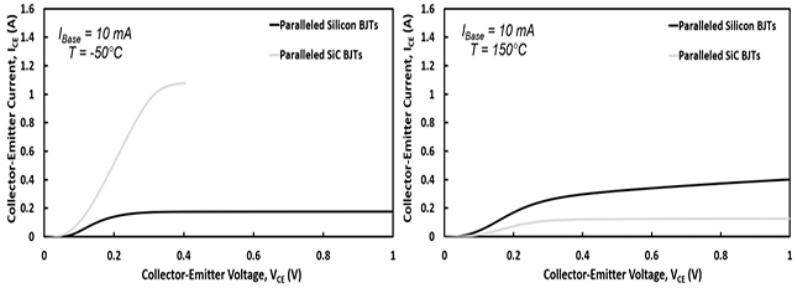

Fig. 6. I-V characteristics of paralleled Silicon and SiC BJTs at I_{Base} of 10 mA at -50°C & +150°C.

Static DC Current Gain

In terms of current gain for paralleled devices as observed in Fig. 7, the current gain of paralleled Silicon BJT is slightly lower than that of single BJT under low temperatures but higher current gain under high temperatures. This is because the improvement in current gain becomes evident at high temperatures. In contrast, the paralleled SiC BJTs lead to the lower current gai

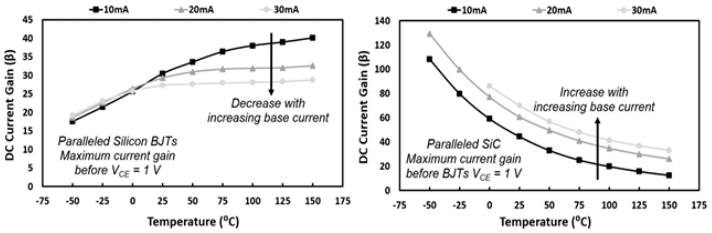

Fig. 7. Common-Emitter current gain for Paralleled Silicon BJTs and SiC BJTs.

On-State Resistance

Fig. 8 shows the on-resistance of two-paralleled Silicon BJTs under various temperatures different collector currents. The parallel connection leads to reduction of on-resistance compared with Single Silicon BJT. A turn-around of measurements is seen in Silicon BJTs where the resistance first slightly increases with temperature between -50°C to 0°C at low base current and then drops with further increase of temperature. This is because at low base current and low temperature the impact of additional carrier generation by temperature is critical, however, as the temperature rises the role of reduced lifetime and mobility by scattering between carriers becomes more effective.

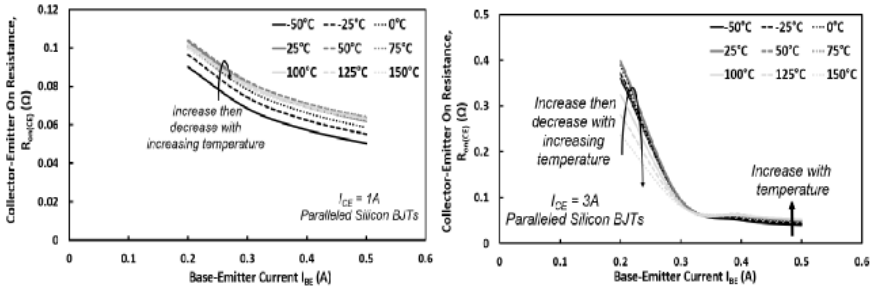

Fig. 8. On-state resistance for paralleled Silicon BJTs at I_{CE} of 1 A & 3 A in different temperatures.

Fig. 9 shows the on-resistance of two-paralleled SiC BJTs under various temperatures at different collector currents. Parallel connection of SiC BJTs can reduce the on-resistance when compared with Single SiC BJTs. This is more pronounced in comparison with single Silicon BJT at low base current. Parallel-connected SiC BJTs introduce the stronger negative temperature dependence of onresistance, albeit it occurs only at low temperatures ranging from -50°C to 0°C.

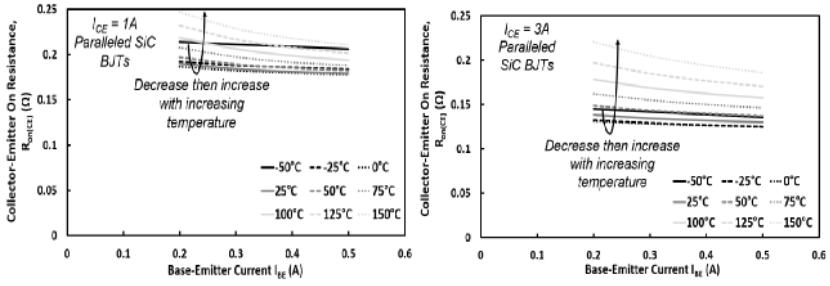

Fig. 9. On-state resistance for paralleled SiC BJTs at I_{CE} of 1 A and 3 A in different temperatures.

The turn-around seen is similar to the Silicon BJT, where at low base current and low temperature the impact of additional carrier generation by temperature becomes more critical, though with the rise of

temperature the role of reduced lifetime and mobility by scattering becomes more effective. The on-resistance of paralleled Silicon BJT is found to be smaller than that of paralleled SiC BJTs at a collector current of 1 A. The decrease of on-resistance with base current for paralleled Silicon BJTs, as shown in Fig. 10, indicates the gradual transition between the active mode and the quasi-saturation mode of operation. In general, parallel connection can promote the conductivity of both Silicon and SiC BJTs especially at elevated temperatures and at low base currents, where the on-resistance of single Silicon BJT at Ibase of 0.2 A under 150°C is reduced by 1.36 Ω when connected in parallel. In essence, the same trends seen for a single SiC BJT can be observed for the paralleled devices too, with the caveat that the base current is divided between two devices, leading to higher resistance per device and there is a slight decreasing trend with the base current.

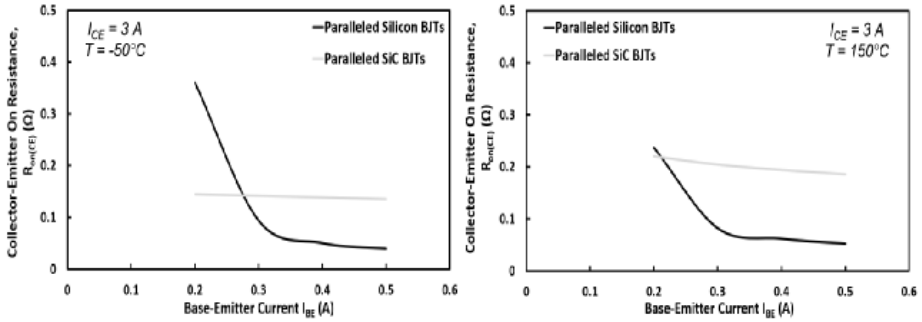

Fig. 10. Comparison of the on-state resistance of paralleled Silicon and SiC BJTs at Ic of 3 A under -50°C and +150°C.

Forward Transfer Characteristics

To characterize the forward transfer characteristic, the Collector-Emitter current (ICE) is measured while sweeping the Base-Emitter voltage (VBE) from 0 to 4 V in 0.05 V increment while fixed Collector-Emitter voltage (VCE) of 0.3 V is used. The temperature is increased from -50°C to 150°C and the forward characteristics are measured and plotted. Fig. 11 and Fig. 12 show the transfer characteristic measured for the Silicon BJT and SiC BJT under various chamber temperatures for paralleled devices. Both Silicon and SiC devices exhibit a lower built-in voltage at high temperatures since the intrinsic carrier concentration increases with temperature, while the temperature from -50°C to 150°C reduces the Base-Emitter voltage by 0.4 V in both cases of Silicon and SiC devices, though this has a more pronounced impact on the Silicon device due to its low base voltage.

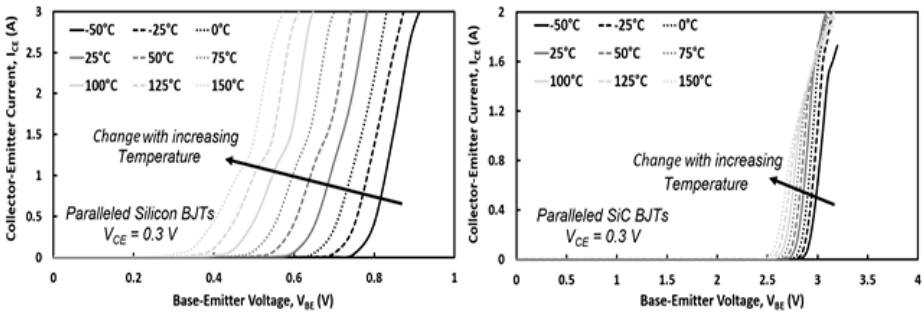

Fig. 11. Forward transfer characteristics of paralleled Silicon & SiC BJTs in different temperatures.

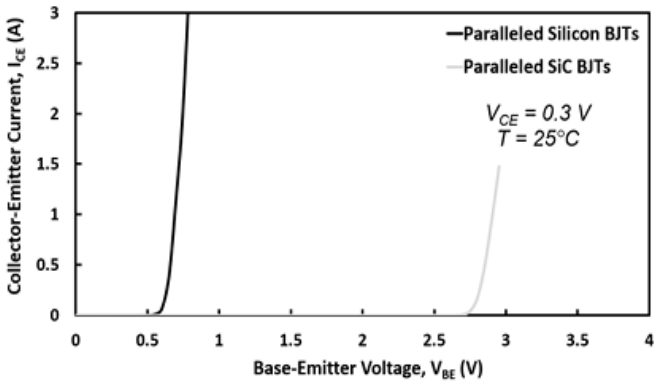

Fig. 12. Transfer characteristics of Silicon vs. SiC BJTs in paralleled connection.

Reverse Base-Emitter Leakage Current

To determine the voltage blocking capability of the Base-Emitter junction, the reverse BaseEmitter current (IRBE), which is also referred to as the Base-Emitter current (IEB), is measured when sweeping the Base-Emitter voltage from 0 to 20 V in the negative direction. The collector terminal is open-circuited. The measurements are done between -50°C to 150°C for paralleled devices.

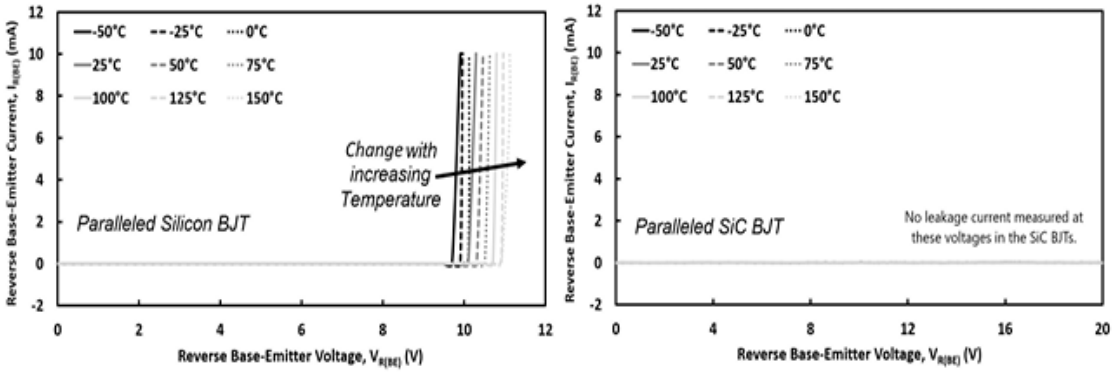

Fig. 13. Base-Emitter leakage current for paralleled Silicon and SiC BJTs in different temperatures.

Fig. 13 and Fig. 14 show the reverse Base-Emitter current of Silicon BJT and SiC BJT under various chamber temperatures for paralleled devices. The positive temperature dependence of the breakdown voltage of Silicon BJTs can be explained by the fact that the movement of free carriers is restricted by the collision with atoms at high temperatures [9, 10], which in turn generates less electron-hole pairs and thus less leakage current, noting that in Silicon almost all dopants are ionized in room temperature.

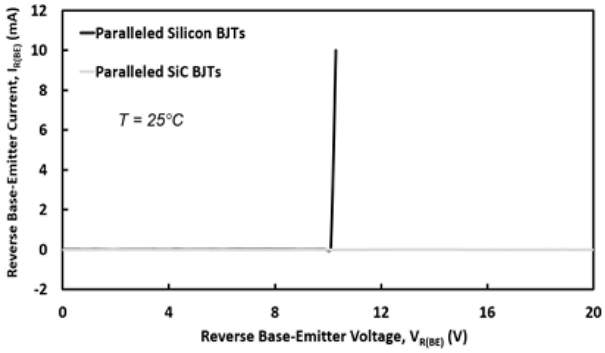

Fig. 14. Base-Emitter leakage current of Silicon vs. SiC BJTs in paralleled connection.

Applications

In applications, current imbalance between paralleled BJTs can lead to reliability problems. Minor differences in the thermoelectrical parameters of the individual devices always exists even if they are fabricated in the same batch. The low-resistance device in parallel connection attracts more current, becomes hotter, and conducts even more current if it exhibits a PTC for current gain (or NTC for onresistance), while the cooler device conducts less [11]. Such positive feedback can result in thermal runaway until destruction. Here it is shown that the current gain of Silicon BJT has improved at high temperatures. Thanks to the parallel connection, the current gain and the conductivity of Silicon BJTs are further enhanced together with their temperature coefficient. However, SiC BJTs are favorable for long-term operation since the negative temperature coefficient counteracts the decrease of onresistance with temperature and thus suppresses the current imbalance between parallel devices.

Summary

Parallel connection is found to promote both the conductivity and current gain for Silicon devices. This also leads to lower on-resistance in parallel SiC BJTs when compared with the single device whereas the current gain is reduced in parallel configuration. Nevertheless, SiC BJT may become preferable to be connected in parallel from the reliability point of view since the negative temperature dependence of on-resistance suppress the current imbalance and thermal runaway.

Acknowledgements

This research article is based on the PhD dissertation/thesis by Chengjun Shen submitted to the University of Bristol in the UK, with online access link to the thesis available on: https://researchinformation.bris.ac.uk/ws/files/383491217/Final_Copy_2023_12_05_Shen_C_PhD.pdf, validated by collaboration with the Compound Semiconductor Applications Catapult (CSAC) in Newport, UK, funded as part of the EPSRC Catapult Network's 'Innovation Launchpad Network+' program with grant EP/W037009/1 and partly funded by the UK EPSRC grant EP/Y000307/1.

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Titanium Nitriding: A Systematic Literature Review

Aria Wira Yuda1,a*, Amir Arifin2,b, Irsyadi Yani2,c and Barlin Oemar2,d
1Doctoral Program, Faculty of Engineering, Sriwijaya University, Bukit Besar, South Sumatera, Indonesia
2Department of Mechanical Engineering, Sriwijaya University, Bukit Besar, South Sumatera, Indonesia

ABSTRACT

In the last twenty years, the manufacturing of titanium and its alloys for commercial use continued to expand. As this material has several very advantageous properties, leading to increasing applications in various industries, it is seldom used in mechanical engineering applications due to its tribological properties, which are unfavourable. The nitriding process is one of the most frequently used thermochemical processes designed to enhance the surface characteristics of titanium alloys and improve tribological properties. Various types of nitriding for titanium are studied, such as ion nitriding, plasma nitriding, laser nitriding and gas nitriding. This article provides a comprehensive examination of research papers on different advancements through a systematic literature review conducted in the period 2017-2023 about titanium nitriding for its process parameters, characteristics and functionalities of the product, particularly emphasising their contributions in surface characteristics and mechanical properties. The review seeks to offer an understanding of how the predominant processing factors, specifically temperature and time, affect the microstructure and the creation of novel phases. This review suggests a challenge for future researchers to investigate mechanisms of microstructure evolution and its impact on mechanical properties in conditioned environments to microhardness and ability to withstand rusting of titanium and its alloys.

Keywords: Titanium, Nitriding, Hardness, Mechanical Properties.

Introduction

Titanium alloys possess a distinctive blend of favourable mechanical properties, lightweight, excellent resistance to corrosion, and biocompatibility, rendering them appealing options for both structural and biomedical uses [1, 2, 3]. However, two significant disadvantages are the increased expense and reduced ease of machining [4]. Titanium alloys, particularly when subjected to sliding contact, are known for their unfavourable tribological properties, such as a high and unpredictable coefficient of friction, significant adhesive wear [5], susceptibility to wear [6], and a strong tendency to jam. Titanium alloys tend to deteriorate when they come into contact with other substances while subjected to pressure, leading to insufficient resistance against both abrasive and adhesive wear [7, 8]. This poses a significant obstacle to the utilisation of Titanium-based alloys for use in tribological applications [9, 10].

Numerous approaches have been formulated over recent years to enhance the durability and hardness of titanium alloys [11]: nitride surface coating by PVD [12]; oxygen or nitrogen thermodiffusion treatment [13]; surface modification through ion implantation [14, 15] and plasma nitriding [16, 17, 18]; laser or arc nitriding [19].

The heat treatment of a titanium alloy leads to alterations in the microstructure and heterogeneity of the material, subsequently causing changes in its properties [13, 20, 21]. The alteration of the surface oxide is bound to occur, possibly changing the corrosion resistance [22].

Therefore, figuring out the progress of research trends in the last five years is worth knowledge that can drive researchers, practitioners/industrial, and universities. The present research aims to identify recent research on titanium nitriding by evolution mechanisms of microstructure and its mechanical properties.

Research Methodology

A systematic method is used to perform the review. A systematic review is a particular approach that identifies and examines available literature, studies, screenings, and analyses contributions, then combines data and reports in order to reach conclusions. It was conducted in a definite manner to select records and the appropriate screening of articles. The pattern used in this study for SLR is depicted in Figure 1. (PRISMA Flow Chart). This will only be achieved if research questions related to the research objectives have been identified.

Research Questions. Titanium nitriding is a process to improve titanium surface by introducing nitrogen ions to form a nitride layer. Nitrogen is highly soluble in a-Ti, thereby strengthening the outermost layer, which has a significant impact [21]. The nitriding process can cause a layer of TiN compounds on top and Ti2N below it, with a hardness that can reach 3000 and 1500 HV. Nitriding cannot be achieved in an open atmosphere due to the appearance of oxygen, resulting in TiO2 formation.

The last decade's research on titanium nitriding mainly focuses on the effect of nitriding process parameters (nitriding temperature, duration, and gas pressure). It has been reported that high nitriding temperature would enhance the diffusion kinetics and increase the nitriding layer thickness as well as the mechanical properties of materials, such as ultimate tensile strength, yield strength, bendability, modulus of elasticity, % reduction in area, hardness, toughness, and % elongation, are also influenced by the hardiness of their surface.

Therefore, the primary aim of this review was to refine the insight into the performance of titanium nitriding. The research goals and corresponding inquiries for this study are outlined in Table 1.

Table 1. Objective and research questions

No	Objectives	Questions
1	To identify the pretreatment process to obtain optimum grains on the titanium surface	What are the distinguishing properties between the most pretreatment parameters used in titanium nitriding?
2	To identify recent research on titanium nitriding diminishes the endurance capacity of titanium alloys	How do process parameters affect fatigue strength?
3	To verify methods to obtain fewer defects and oxygen content in the nitride layer	How has nitriding method variance been affected by defects and oxygen content?

Search Strategy and Criteria. TITLE-ABS-KEY (titanium AND nitriding) AND (LIMITTO (PUBYEAR , 2023) OR LIMIT-TO (PUBYEAR , 2022) OR LIMIT-TO (PUBYEAR, 2021) OR LIMIT-TO (PUBYEAR, 2020) OR LIMIT-TO (PUBYEAR, 2018) OR LIMIT-TO (PUBYEAR , 2017). The search strategy used in this review is concentrated on five resources find journal articles and publications relevant to the scope of the paper. The database was selected because this scientific database is highly extensive and thorough, encompassing a diverse array of data, thereby inspiring progress and advancement of meaningful bibliometric investigations. Other sources, such as "JStor" and "IEEE Xplore", were utilised to obtain additional records. In terms of search standards, this review covers the period from 2017 to 2023, including further studies, considering that some titanium nitriding applications are still being examined for use in to improve material and structure quality.

To obtain a titanium nitriding investigation of the scientific community, the subsequent step the process of conducting a literature search involves incorporating two distinct phases within the document search: TITLE-ABS-KEY “titanium” AND “nitriding”. The word "steel" is not employed due to the word’s

frequent usage by numerous authors across articles. Ultimately, the author decided to conduct a search using the "Title" criterion in order to locate precise articles within the scientific community that concentrate on titanium.

Screening. The screening phase in this review commences by removing duplicates. As we examined three electronic databases and two more, numerous instances of repetition were discovered. After eliminating duplicate records, the remaining ones are carefully examined to find relevant studies. At this moment, the subsequent categories are eliminated: Reports, Book Chapter, Thesis, Proceeding, Newspaper/ Magazine Articles, and No Access to Full Text. After removing duplicates, the remaining records are selected for relevant content.

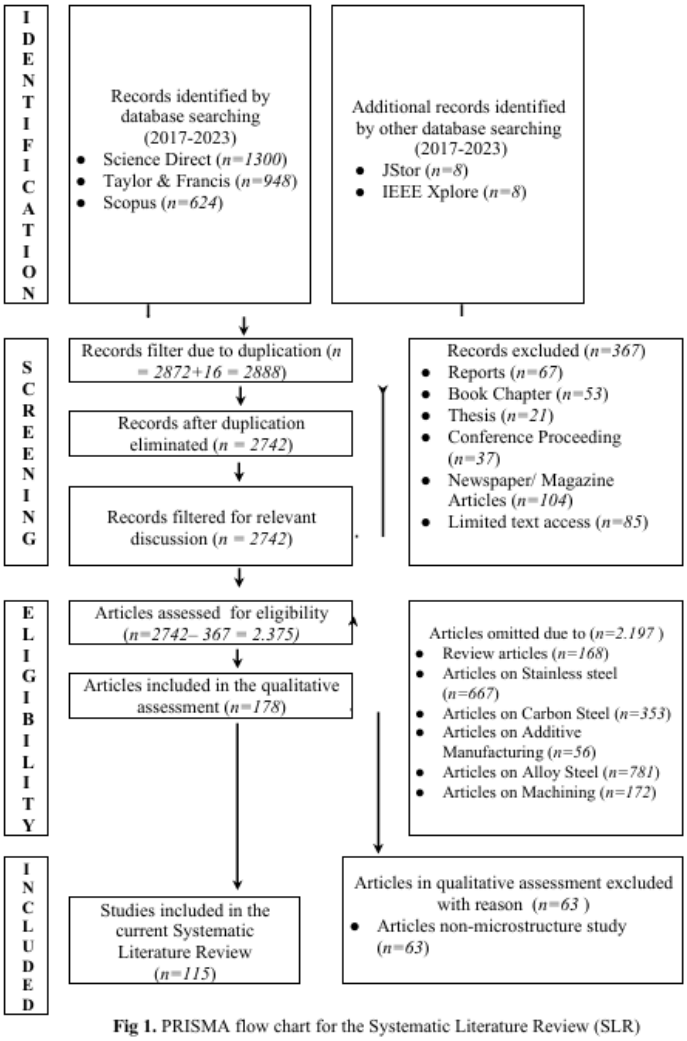

Fig 1. PRISMA flow chart for the Systematic Literature Review (SLR)

Inclusion and Exclusion Criteria. In this review, we conducted an extensive search in order to find the most significant research articles to be utilised in the Systematic Literature Review (SLR). Exclusion of Review articles, Articles on titanium nitriding without Stainless steel, Articles on Carbon Steel, Articles on Additive Manufacturing, and Articles on Alloy Steel without nitriding are the basis for selecting the articles. The purpose of the inclusion and exclusion process is to choose appropriate studies to analyse the required data.

Data Analysis

Scientific records in the use of nitriding method for titanium during 2017-2023 maintained the same trend with technological advances. But, one interesting thing is that during the period, a wide range of

methods of titanium nitriding properties have been explored. This is possible because this method has been utilised since the early 1980s and is being used until now. Fig. 2 shows that the research on this topic in 2022 had twenty-four (24) articles, with the most number of articles followed by 2021, which had twenty (20) articles. We can also observe that in 2018, there was the smallest number of articles compared to other years.

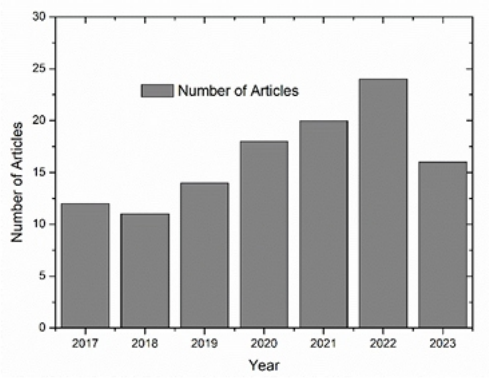

Fig 2. Published articles for 2017-2023

Thirty-one different journals were checked in this SLR. This shows that nitriding is applicable in titanium treatment due to its potential impact on suitability and cost savings. However, only four journal sources published >3 articles; of three sources, the journal with 9 articles was "Surface and Coating Technology". The journal specialises in publishing articles in the field of engineering materials. The second and third most common journals were "The Journal of Manufacturing Processes" and "Material Research", both specialises in publishing research articles in the field of Material. Fig. 3 shows that the journals "Mechanics of Advanced Materials and Structure" and "Material Chemistry and Physics" had eight articles, respectively.

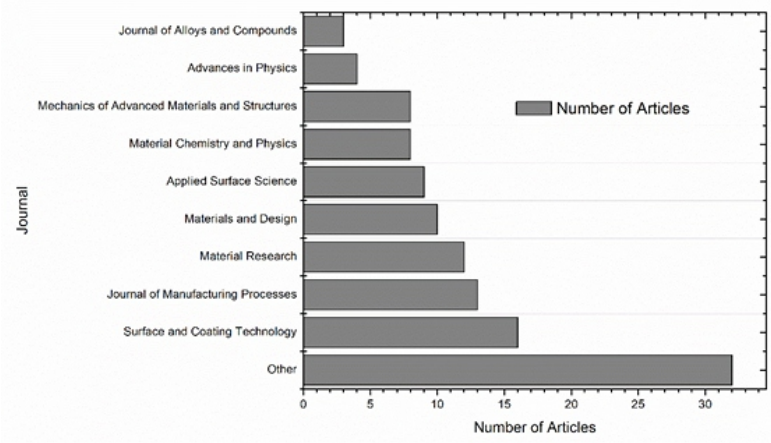

Fig 3. Total articles released per Journal

Geographical aspects of the articles are observed through the utilisation of content analysis. Even though articles are not explicitly labelled with keywords, content analysis is conducted to classify them based on their respective locations. It is intriguing to note that various nations are engaged in researching the process of nitriding titanium. Twenty countries around the world were found. P.R. China, Russia and India with twenty-six (26), seven (7), and seven (7) articles, the highest number of published articles in this study belong to these three major countries, in the order stated above (see Fig. 4).

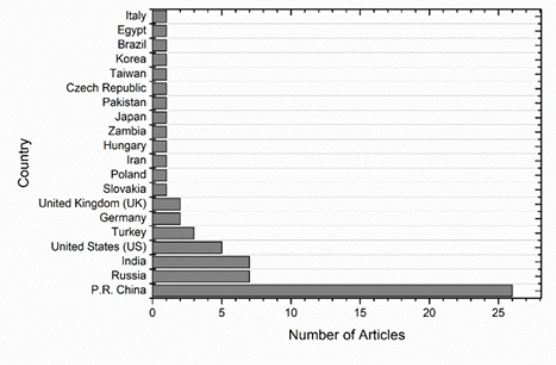

Fig 4. Articles on Titanium Nitriding published per Country

Trends by country activity present that P.R. China is still the most active and predominant carrying research among all countries. The United States published five (5) articles; Turkey published three (3) articles; India, Germany and the United Kingdom each published two (2) articles. At the very least, there are countries which only publish one article of each. They are Slovakia, Poland, Iran, Hungary and Italy.

Nitriding

Nitriding is featured by layer formation due to the use of temperature, and then nitrogen is transferred to the surface. Therefore, various research were performed to study the effects of temperature on mechanical properties [23] and microstructural change. The nitriding process for titanium treatment has recently been researched by Hanyang University, Nippon Steel and Sumitomo Metal Corporation, Wuhan University of Science and Technology, and other institutes, groups, as well as universities. The nitriding process has been progressed by laboratory research, and a new plasma nitriding process has been made for small specifications.

Table 2. Summary of the research on hot-roll by temperature

Author	Year	Main Focus	Material studied	Process parameter	Properties examined
[24]	2017	Two-stage laser plasma nitriding	Pure titanium	- case hardened	- case hardness value - case depth
[25]	2019	Sputtering technique (deposition)	Titanium	-coating deposited for different times	- corrosion behaviour - tribocorrosion test
[26]	2017	Diffusion hardening by vacuum rapid nitriding	Pure titanium	- pre-heat treatment with interval 10°C at temp 700-800°C	-depth of hardened layer - friction resistance
[27]	2023	Gas nitriding	Ti-6Al-4V	- gas nitriding by 99,99% purity of nitrogen at 1073°K	-microhardness -thickness of nitriding layer
[28]	2017	Laser nitriding in an open atmosphere	Pure Titanium Gr. 2	- 40W laser power - 25 mm/s scanning speed - 1,5mm standoff distance - 5 bar N_2 pressure	-microstructure -surface color -morphology
[29]	2021	Post-heating in the N_2 atmosphere using a tubular furnace	Ti-6Al-4V	-heated into 900°C with heating rate 7°C/min, cooled to room temp. for 4h	- coated layer thickness - surface texture
[30]	2021	Laser nitriding	Ti-6Al-4V	-Power output 1-4kw, - Nitrogen with high purity (99.9%) as well as a mixture of gas consisting of equal parts Nitrogen (50%) and Argon (50%)	- State ionisation of nitrogen - N layer - nitrogen and oxygen levels on the surface
[31]	2018	Cathodic arc deposited titanium nitride	Ti-6Al-4V	- Exposing the material to Nitrogen of exceptional purity, operating at a specified pressure of 3Pa for 60 minutes for nitriding	-Wear rate -Scratch test
[32]	2022	Gas nitriding	Pure titanium	- treatment in a nitrogen atmosphere at 900°C	-Thickness of TiN layers - composition of titanium nitrides and oxides - roughness
[33]	2021	Vacuum inductive nitriding layer	Titanium alloy	-Temp. T = 850 °C - Pressure 30kPa for 60 min in N_2	- abrasion loss - wear performance
[34]	2018	RF magnetron sputtering	Pure titanium	-A combination of Ar (99.999%) flowing at a rate of 15 cm^3/min and N2 (99.999%) flowing at a rate of 2 cm^3/min	-TiN films observation
[35]	2022	Watt-level pulsed laser nitriding	Pure Titanium	-laser 4.2W with pulse 10Hz and 5 ns	-Thickness of nitride layer -Surface hardness
[36]	2023	Cathodic cage plasma nitriding	Pure Titanium	-chamber evacuated to 10^{-4}Pa prior to administering a gas mixture of N_2 and H_2 - net gas pressure 200Pa for 60 min	-impact of hydrogen on the microstructure and mechanical characteristics
[37]	2019	Electron beam nitriding in vacuum medium	Pure titanium	-vacuum plasma cathode with current up to 100mA and energy up to 8kV	-chemical composition of the nitride layer -microstructure of layer

Microstructure shape characteristics and mechanical tests were undertaken as evidence to demonstrate the impact of temperature on mechanical characteristics [38, 39, 40]. Nitrogen can permeate the titanium base through different processes. One option is to elevate the temperature of the base and expose it to nitrogen gas or ammonia (known as gas nitriding). Another method involves subjecting the base to plasma nitriding, which heats the surface and introduces nitrogen ions into the nitrogen plasma simultaneously [41], which simultaneously heats the surface and provides nitrogen ions to it. Plasma nitriding has the advantage of an inherent sputtering phenomenon. Plasma nitriding offers an extra benefit of the natural sputtering effect, which not only cleans the surface but also diminishes impurities within the nitriding sample. Both gas and plasma do not clean the substrate or reduce impurities in the nitriding sample.

In another study, it has been presented that nitriding resulted from oxygen concentration, which influences surface carbon concentration balanced with the atmosphere. It was also strengthened by experimental and numerical research on the effects of duration on recrystallisation, resulting in hardening. The effect of nitriding temperature that causes the oxide scale was also studied to find the optimum temperature for reducing the thickness of the oxide scale.

Conclusion

This study reviewed 115 papers published by prestigious international publishers 2017-2023 to understand the titanium nitriding research area. Therefore, this article conducted a comprehensive evaluation of previous research papers to improve our comprehension of the titanium nitriding procedure and the impact of different factors on its performance, with a specific emphasis on how they influence mechanical properties.

The significant issues and challenges that stand out are the need for collaborative research in an advanced sequencing process for nitriding schedule and conditioned space to study the effect of an environment on microstructure forming. Titanium nitriding process designs gained as a result of engineering calculations created according to the principles of plastic forming have been made, and defects under simulation using the finite element method were determined before the prototype was produced. This resulted in a reduction in costs for a prototype production study compared to the prior simulation program, according to a review of the literature, modelling and the task of identifying and eliminating hazards in the early stages of the project.

Nowadays, the use of analysis-based testing shows promise as a viable alternative to physical experiments, as it helps to decrease the costs and time required for carrying out such tests. Numerical simulation is an effective way to guide the production process. Still, the application in titanium nitriding processes is immature due to the conditioned environment as a boundary limit for the modelling. Future works should address the complex relationship among process parameters in the conditioned environment to uncover titanium nitriding characteristics that remain challenging to anticipate through analytical models.

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Extraction and Characterization of Cellulosic Fiber from Banana, Sugarcane, and Napier Grass

Showna Lee T. Sales1,2,a*, Virgilio Abellana1,b, Camila Flor Y. Lobarbio1,c
Ian Christopher Dano2,d , Richard P. Balbutin Jr.2,e
1Doctor of Engineering, School of Engineering
University of San Carlos, Talamban, Cebu City 6000, Philippines
2Civil Engineering Department, College of Engineering Education, University of Mindanao, Davao City 8000, Philippines

ABSTRACT

Cellulosic fibers are one of the trend studies being conducted from the recent research due to their cost-effectiveness and abundance as biomass waste products from different plantations. The study aims to fabricate a dew extractor machine and analyze and characterize fibers based on their physical, mechanical, and chemical properties. The machine achieved the required torque, which is 370.645 N.m, and a speed of 28.82 rpm for the initial process for the sources of fiber by using a chain drive. Among the three fibers, the banana shows greater tensile strength with 221.225 MPa - 418.59 7MPa for untreated and 191.376 MPa – 715.428 MPa for treated. Napier has the smallest value of tensile strength with 77.944 MPa – 146.731 MPa for untreated and 76.048 MPa – 287.689 MPa for treated. The chemical properties of the fibers were analyzed using Fourier Transform Infrared Spectroscopy shows all three fibers have a similar single-, triple- and double-bond, namely a secondary aliphatic alcohol, alkene, and a non-conjugated alkene functional group. It can be concluded that treated fibers can withstand more stress, stretch even more, and therefore are more elastic than untreated fibers.

Keywords: Natural Fibers, Physical Characterization, Mechanical Characterization, Chemical Characterization, Dew Extractor Machine, Fourier Transform Infrared (FTIR)

Introduction

Cellulosic Fibers are materials obtained from natural resources such as banana plants, kenaf, Napier, sisal, and other plants. Mainly, these fibers are used in textiles, concretes, and composites. Due to its characteristics that are beyond synthetic fibers (i.e., minimal cost, lightweight, eco-friendly, renewability, recyclability, and biodegradability), a variety of industries use this, including aerospace, construction, defense, and automobiles. Moreover, cellulosic fibers have higher yields, cheaper processing costs, and lower density than synthetic fibers [1]-[4].

The fibers can be extracted in a variety of ways depending on the plant's component sensitivity to degradation and the amount of fibrous material removed. The most common natural fiber extraction processes are dew and water retting [3]–[6], alkali extraction [7]–[9], and mechanical extraction [6] employed by scraping devices [10]. Of which, the most commonly used are dew and water retting in terms of yield. Before utilizing the fibers for industrial use, it is often treated with Sodium Hydroxide (NaOH) to account for their low thermal stability, hydrophilic nature as well as low reactivity with thermoplastic and thermosetting plastic [11]. [8] presents a study that utilizes one such treatment wherein the cellulosic fibers extracted from the stem of Catharanthus roseus (rose periwinkle) undergo

treatment. The treatment enhanced the fibers' tensile strength, crystalline index, and surface roughness, as well as increased the fiber's thermal stability and wettability in the liquid state. As such, the proponents deemed the alkali-treated fibers fit for industrial use, specifically in developing lightweight composites [2],[8].

Among the number of sources of natural fibers, the most common sources are bananas, sugarcanes, and Napier grass plants [12], [13]. This is primarily due to many countries, including the Philippines, having specific plantations dedicated to generating banana and sugarcane products, as well as an abundance in Napier grass growth [14]. These plantations, in turn, produce a lot of biomass waste, such as the pseudo stem of banana, sugarcane, and Napier grass, all of which are found to be good sources of natural fibers [14], [15].

Hence, this paper aims to generally discuss the extraction and characterization of fibers, namely from the pseudo stem of the banana plant, sugarcane, and Napier grass. Specifically, it aims to: (1) fabricate a portable dew extractor machine and (2) analyze and characterize fibers based on their physical and mechanical properties.

The purpose of this paper was to create a database for future research in terms of characterizing the fibers presented. This will likewise serve as a basis of data when analyzing the aforementioned fibers in the reinforcement of building materials such as concrete and composites.

Materials and Methods

The different sources of fibers used in the study were from the Musa balbisiana (Cardava banana) pseudo-stem, which is growing in a nursery stage, 93's-A variety of Saccharum (sugarcane), and Pennisetum purpureum (Napier grass); all of which were abundant in the Philippines.

Dew Extractor Machine. The developed dew extractor machine designed in this study was based on the system and calculations of [16] study about a small-scale sugarcane juice extractor. The machine is composed of four sections which are: feeding and crushing sections, power section, torque and speed reduction section, and frame section. The power section consists of an AC motor which acts as the main power transmitter in the whole system of the machine. All of the components that are mounted and make up the machine system are supported by the frame section.

In order to accommodate the varying sizes of sugarcane and Napier grass, the maximum size of the roller was determined in the reference [17]. The weight of the crushing roller was estimated as a reference from [18]. The density of the crushing roller material is equal to 7840 kg/m3, and the acceleration due to gravity is equal to 9.81 m/s2. The force and torque of the crushing roller were determined in reference [16]. Utilization, calculation, and analysis were considered with reference to [20] in order to obtain the necessary power and speed to operate the machine's entire system. Fiber Testing. Among the three sources of fibers, two of them (Napier grass and sugarcane) are required to undergo a pressing process through the developed dew extractor machine. This was done to ensure that the said sources did not damage the decorticator machine. The fibers were exposed to sunlight to prevent spoilage [22]. The samples were grouped into two: the treated and untreated groups, forming six groups in total. The untreated group was subjected to various tests without any additional alterations to the fiber. On the other hand, the treated groups were subjected to an alkaline treatment using a NaOH solution of 4.5% concentration before testing to increase the fiber's strength, stiffness, and surface roughness [23].

To obtain the linear density of fibers, a single strand was taken from each of the six test groups. The mass and diameter of each strand were measured in order to get the linear density (tex), mass density (ρ), and volume of each fiber. The length of the fiber was kept at 8cm for all observations. Following ASTM D3822/D3822M-14 or the Standard Method for Tensile Properties of Single Tensile Fibers, a random sampling of fibers was obtained from each of the six groups. The samples were taped with only a 1 cm

gap left in between. This process was repeated to over 20 strands of fiber from each of the six groups. Digital compression and tensile machine (UE1501, 1000N, Laryee Instruments Co.) was used with a constant rate of extension of 1.00 mm/min to calculate the breaking force and maximum elongation of each fiber strands. Tensile stress (σ) was calculated by dividing the load applied by the fiber's cross sectional area, and the calculation for strain (ε) can be obtained by comparing the original unstressed length and the subsequent elongation upon failure. Lastly, Young's modulus (E) was calculated by getting the ratio of tensile stress (σ) to tensile strain (ε).
Moreover, the untreated samples of the three fibers were subjected to FTIR analysis using SHIMADZU 8400 machine.

Results and Discussions
Fabricated Dew Extractor Machine. Following the final design presented in this paper, the proponents were able to fabricate a dew-extracting machine. The machine used a sprocket instead of gears considering the availability and cost-effectiveness of the materials. During the fabrication adjustment of the drafted design was encountered, limits and calculations were maximized nor minimized to obtain a functional and economically fabricated machine. Figure 1 shows the actual dew extractor machine.

Fig. 1 Fabricated Dew Extractor Machine

The dew extractor machine is made up of various parts, including a 1.5 horsepower AC motor, a chain sprocket with 13 and 51 teeth, a roller, a chain, shafting, pillow blocks, bolts, nuts, and washers. The 1740 rpm AC motor has an aluminum winding and runs on 220V, 60 Hz. The number of teeth determines the type of sprockets; the idler sprocket has 16 teeth, while the motor and shafting sprockets have 13 teeth. To achieve high torque, the 13 teeth are always paired with 51 teeth. For the roller to rotate into a different motion, the idler sprocket is used. The frame was constructed using a mild steel 1" by 1" angle bar and 2 mm plain sheet for its high impact strength, toughness, weldability. The roller is constructed of mild steel schedule 40, which can handle more compressive stress. The driven shafts have 443.529 rpm and 113.0564 rpm and the maximum torque of 24.0827 N.m and 94.4782 N.m, respectively. The actual speed of the crushing rollers is 28.82 rpm with a 370.7 N.m maximum torque which is enough to press and extract the dew of the sugarcane and Napier grass. Fiber Property Characterization. This section covers the findings of the three fibers, which divided into treated and untreated groups based on their physical, mechanical, and chemical characteristics. Physical Property Characterization. The physical properties of each fiber sample, such as the diameter, linear density, and density, are summarized in Table 1 for the untreated group and Table 2 for the treated group, respectively. As presented in Table 1, USF shows the largest values for diameter, with values ranging from 0.227mm to 0.393mm. As for the fiber's linear density, USF also has the largest magnitude with values ranging from 0.0570g/m to

0.1236g/m, followed by UNF having a range of 0.0096g/m to 0.0380g/m and UBF with a range of 0.0123g/m to 0.0191g/m the smallest. Lastly, for the density of the fibers, USF has the biggest values with ranges from 1.0013g/cm3 to 1.5189g/cm3, and UNF is in the smallest with a range of 0.8559g/cm3 to 1.3879g/cm3.

Table 1 Physical properties of untreated natural fibers

Natural Fiber	Diameter (mm)	Linear density (g/m)	Density, (g/cm^3)
Untreated Banana Fiber (UBF)	0.109 - 0.151	0.0123-0.0191	0.9230-1.3440
Untreated Napier Fiber (UNF)	0.110-0.210	0.0096-0.0380	0.8559-1.3879
Untreated Sugarcane Fiber (USF)	0.227-0.393	0.0570-0.1236	1.0013-1.5189

Table 2 Physical properties of treated natural fibers

Natural Fiber	Diameter (mm)	Linear density (g/m)	Density, (g/cm^3)
Treated Banana Fiber (TBF)	0.067-0.093	0.0798-0.0802	2.4176-3.6270
Treated Napier Fiber (TNF)	0.206-0.262	0.0467-0.0736	1.1268-1.6853
Treated Sugarcane Fiber (TSF)	0.232-0.323	0.0539-0.1097	1.0648-1.6074

Table 2 shows that TSF has the largest diameter and linear density ranging from 0.232mm to 0.323mm and 0.0570g/m to 0.1236g/m, respectively. TBF has the biggest mass density among all three fibers with a value of 2.4176g/cm3 to 3.6270 g/cm3. The result shows that sugarcane fibers have the largest diameter and linear density in both treated and untreated samples, while banana fibers have the smallest values in both treated and untreated samples. In terms of raw density, TBF showed the greatest value, while UBF showed the smallest. As for the differences between the treated and untreated samples, an effective change can be observed in the density of the fibers. This is especially evident in the banana fibers, which had the greatest change from a maximum density of 1.3440g/cm3 while untreated to a maximum density 3.6270g/cm3 after treatment. Banana fiber is significantly impacted by treatment, which reduces its diameter. After treatment, the linear density and density of all fibers increase. The mass of the is considerably affected when the fiber's diameter decreases. As a result, the increase of linear density and density will decrease the mass of the fibers as the length remains constant. This indicates that fibers reduced their possible tensile strength.

Mechanical Property Characterization. The mechanical properties of both untreated and treated groups of fiber, such as its single tensile stress, elongation, and Young's modulus were summarized in Table 3 and Table 4 respectively.

Table 3 Mechanical properties of untreated natural fibers

Natural Fiber	Single tensile (MPa)	Elongation (mm)	Young's modulus (GPa)
Untreated Banana Fiber (UBF)	221.225 - 418.597	0.4312 - 1.0550	2.799 - 7.123
Untreated Napier Fiber (UNF)	77.944 - 146.731	0.3776 - 1.0006	1.076 - 3.315
Untreated Sugarcane Fiber (USF)	121.524 - 250.921	0.5733 - 1.0235	1.686 - 4.609

Among the untreated fiber groups, as shown in table 3, UBF can withstand the most load at around 221.225MPa up to 418.597MPa. This was followed by the USF with 121.524MPa to 250.921MPa, and lastly, the UNF, which can only withstand 77.944MPa up to 146.731MPa before breaking. In terms of elongation, all three fibers stretched similarly up to a certain point before breaking. UBF has the greatest elongation ranging from 0.4312mm to 1.0550mm. In terms of the modulus of elasticity, UBF had the

greatest magnitude with a range of 2.799GPa to 7.123GPa.

Table 4 Mechanical properties of treated natural fibers

Natural Fiber	Single tensile (MPa)	Elongation(mm)	Young's modulus (GPa)
Treated Banana Fiber (TBF)	191.376 - 715.428	0.3723 - 0.6589	3.868 - 14.249
Treated Napier Fiber (TNF)	76.048 - 287.689	0.5081 - 1.2111	1.035 - 3.459
Treated Sugarcane Fiber (TSF)	83.423-314.633	0.6756 - 1.5452	0.898 - 3.530

As for the treated sample group, presented in table 4, TBF can withstand the most load among the three at around 191.376MPa up to 715.428MPa. For elongation, unlike the untreated samples, there was a significant difference between the elongation capacity of the three fibers. TSF had the greatest elongation, followed by TNF and TBF to be last in order. Lastly, in terms of the modulus of elasticity, TBF had the most significant values with a range of 3.868GPa to 14.249GPa. Of the three fibers, the treated fiber showed the highest change in single tensile strength, which is a favorable sign for application. Furthermore, banana fiber's Young's modulus increases noticeably after being treated with sodium hydroxide [24], whereas Napier and sugarcane fiber's Young's modulus decreases. In addition, sugarcane and Napier both had a low young's modulus, which is a sign of brittle fiber. The banana, on the other hand, has the greatest tensile and young's modulus value and is, therefore, the most elastic to them. Chemical Property Characterization. A summary of the analysis of the chemical properties of the banana, napier grass and sugarcane fibers from the Fourier Transform Infrared analysis results was shown below.

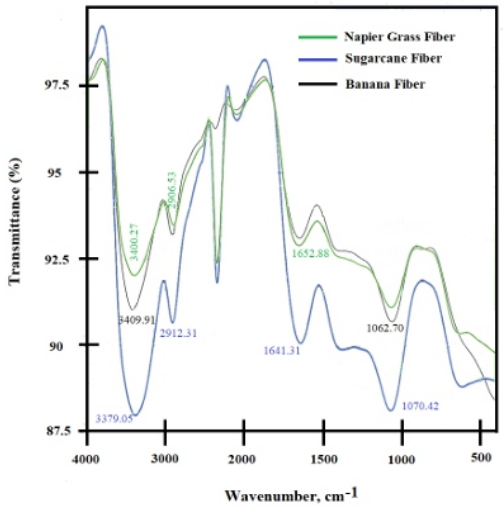

Fig. 2 FTIR spectra of Banana, Napier Grass and Sugarcane fiber

As presented in Figure 2, all fibers show similar characteristics in terms of the absorption of the infrared spectrum. In terms of ts functional groups, all three fibers show a similar single-, triple- and double-bond, namely a secondary aliphatic alcohol (O-H), alkene (C-H), and a nonconjugated alkene functional group, with peak values of 3300-3500 cm-1, respectively. As for the fingerprint region, both Napier and sugarcane fibers contain the primary aliphatic alcohol and distributed alkene (R'HC=CHR), while the banana fibers only have the primary aliphatic alcohol at their fingerprint.

Conclusion

In this study, a design for a machine that extracts dew from sugarcane and Napier grass was developed and fabricated. Based on the results, the machine was found to be functional, economical, and efficient

in doing its intended purpose. In terms of fiber testing, the results showed that treating the fibers leads to significant changes to their physical and mechanical properties. In terms of physical changes, the diameter of the fiber often reduces while its mass stays almost the same. On the other hand, the density of the fiber increases. As for the mechanical properties, it can be concluded that treated fibers can withstand more stress, stretch even more, and therefore is more elastic compared to the untreated fibers.

As for the various sources of fibers, in terms of their chemical composition, all three fibers have the same composition with a small exception on the fingerprint region of the banana fibers as it only has one in contrast to the others, which had two. Among the three fibers, the results showed that the banana fiber has significant great changes in all aspects. It increases its magnitude for tensile, young's modulus, density, and linear density. In contrast, it decreases the diameter and mass of the fiber while the length remains constant. Furthermore, the banana fibers are also the most elastic among the three despite having the smallest diameter. The sugarcane comes second, and the Napier grass is found to be the least elastic. As such, it can be concluded that banana fibers are a viable additive in concrete strengthening.

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Impact of Single-Step Deep P-Body Implant on 1.2 kV 4H-SiC MOSFET

Pavan Vudumula1,a, Yu-Chieh Chien1,b, Abdul Hannan Yeo1,c*, Lakshmi Kanta Bera1,d, Umesh Chand1,e, Voo Qin Gui Roth1,f, Surasit Chung1,g, Navab Singh1,h, Yee-Chia Yeo1,

1 Institute of Microelectronics (IME), Agency for Science, Technology, and Research (A*STAR), Singapore 138634.

ABSTRACT

In this work, TCAD simulation of SiC MOSFETs design with deep (2 μm) p-base single step aluminum channeling implant along [0001] direction and JFET design using phosphorus implant is presented. The threshold voltage (Vth) was around 3 V for both the devices. Improvements to the specific on-resistance (Ron,sp) reduction by ~ 30 %, breakdown voltage (BV) enhancement by ~ 40 %, miller plateau (QGD) reduction by ~ 30% is reported. Furthermore, both the Baliga figure-ofmerit (BFOM) (BV2/Ron,sp) and high-frequency figure-of-merit (HFOM) (Ron,sp × QGD) with 2 μm deep p-base /JFET implant are enhanced as compared to shallow 0.7 μm p-base/JFET implant. This paper provides valuable insights into the advantages of a single-step channeling implant at room temperature, without the need for a hard mask. This approach offers a high throughput with a lowcost process for fabricating high-performance SiC MOSFETs.

Keywords: Channeling implant, Deep p-body, Single step implant

Introduction

4H-SiC MOSFETs are well-suited for hybrid electric vehicles (HEV) and pure electric vehicles (EV) with a voltage rating of 1.2 kV. This is attributed to their impressive BV, low Ron,sp, and fast switching speeds [1]. These devices consist of box-shaped implantation profiles formed through multi-step processes, including the p-base, JFET, n+ and p+ regions. Aluminum is used for both the p-base and p+ implantation, while phosphorus is used for the JFET and n+ implantation [2]. The multi-step implantation for box profiles is commonly conducted utilizing SiO2 hard masks at high temperatures (> 400 °C). Undoubtedly, this process entails several steps that inherently impede manufacturing throughput. Few studies have investigated the impact of deep p-body and deep JFET on Ron,sp, BV and short circuit withstand time [3,4]. A recent study has shown that a well-defined box-type profile can be achieved through a single-step implantation with significant depth along the [0001] and [112 $\bar{3}$] crystal orientations [5]. However, the box shape profile is more effective in the [0001] direction. The channeling implantation process performed at room temperature, allows the use of photoresists which eliminates the need for hard mask processes. This helps to streamline fabrication by eliminating several steps involved in hard mask patterning which could lead to significant cost reductions. This channeling implant has potential applications in SiC super junction devices too. However, there are little reports on the characteristics of deep p-body standard SiC MOSFETs using single-step implant. This study investigates the impact of a deep p-body using a single-step implant profile along [0001] and the corresponding JFET implant design using phosphorous implant along [0001] in 1.2 kV MOSFETs in terms of its static and dynamic characteristics.

Results and Discussion

Experimental data on aluminum channeled implantation with an energy of 300 keV and a dose of 1.2×1013 cm-2 along the [0001] crystal direction show a nearly box-shaped profile up to a depth of 2 µm [4]. This profile has been used for the p-body. To achieve a uniform JFET design, phosphorus implantation with optimized parameters (energy: 300/500/700 keV, dose: 3×1012/3×1012/ 1.2×1013 cm-2) is necessary. The implant profile is illustrated in Fig. 1.

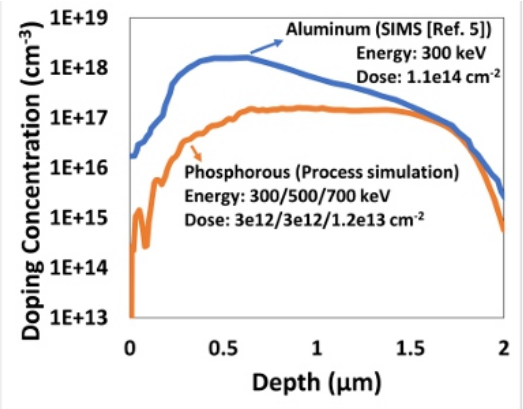

Fig. 1 Simulated doping profile for deep (2.0 µm) channeling implantation along [0001] orientation with optimized JFET profile.

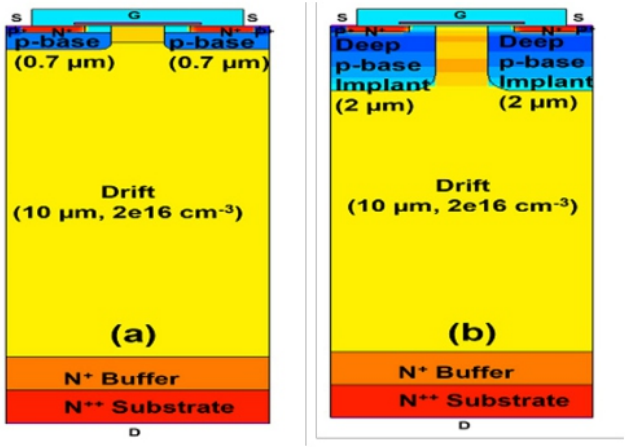

Fig. 2 Schematic of (a) non-channeled 0.7 µm p-base and (b) channeled single-step implanted 2 µm p-base from TCAD simulation.

he device cross-section of a 1.2 kV MOSFET with a non-channeled implant for a p-body depth of 0.7 µm and a p-body depth of 2 µm using channeling implant is depicted in Fig. 2 (a) and (b), respectively. These devices are simulated using TCAD with WJFET = 1 µm, Lch = 0.5 µm, Ldrift = 10 µm, and a uniform epitaxy doping profile of 2 x 1016 cm-3. The extracted threshold voltage (Vth) is approximately 3 V for both devices, and specific on-resistance (Ron,sp) from Id-Vd characteristics (Fig. 3 (a)) is 30% lower with a JFET implant depth of 2 µm compared to a shallow JFET implant depth of 0.7 µm. This reduction is due to 2 µm charge sustaining layer (CSL) with deep JFET implant, resulting in increased electron flow and thus a lower Ron,sp. Fig. 3 (b) demonstrates a 40% improvement in blocking voltage for the p-body device with a depth of 2 µm compared to the device with a depth of 0.7 µm. Enhanced two-dimensional electric field distribution with deeper p-body compared to shallow p-base allows the device to sustain higher blocking voltages. Deep p-base better shields the channel and gate oxide from high drain bias due to the depletion in JFET.

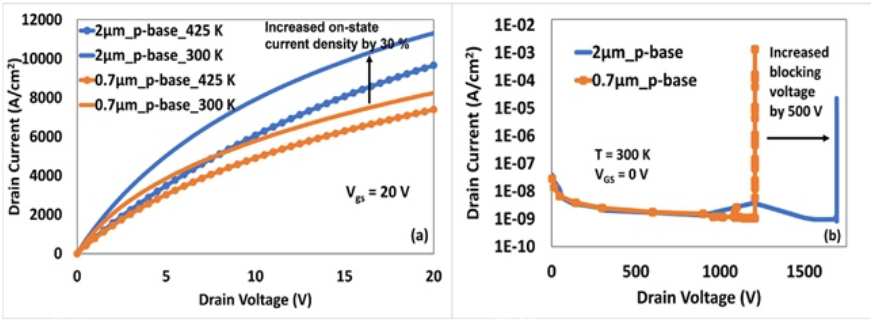

Fig. 3 Simulated (a) output and (b) blocking voltage characteristics for SiC MOSFETs with non-channeling (orange) and channeling (blue) implantation.

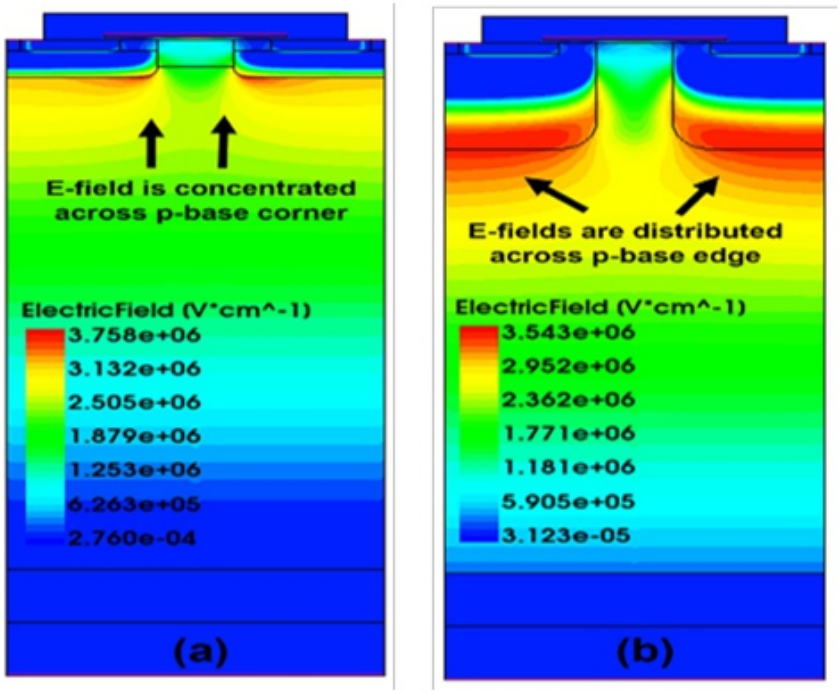

Fig. 4 Blocking-state electric field distribution near breakdown for (a) non-channeling 0.7 μm and (b) channeling 2.0 μm p-base region in SiC MOSFETs.

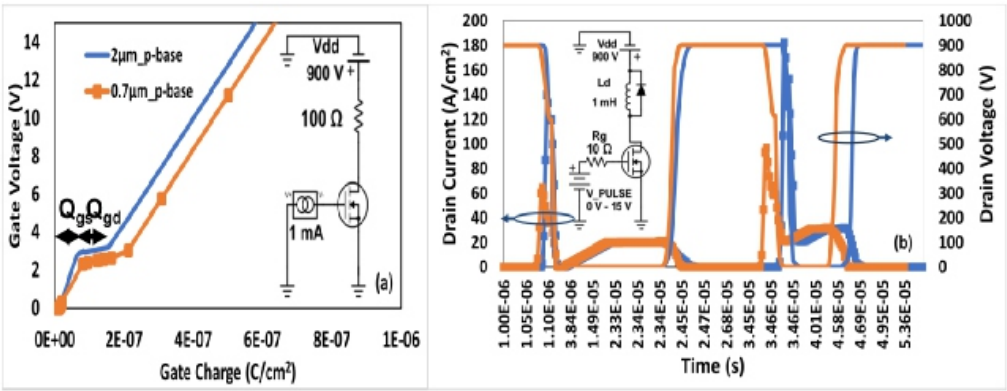

Fig. 5 Simulated (a) gate charge and (b) switching characteristics with non-channeling 0.7 μm and channeling 2.0 μm p-base region in SiC MOSFETs.

The off-state electric field distributions near the breakdown regime for 0.7 µm and for 2 µm p-base are shown in Fig. 4 (a) and 4 (b). Additionally, gate charge (Fig. 5(a)) and clamped inductive load switching simulations (Fig. 5 (b)) are performed using a mixed-mode SPICE environment to analyze the miller plateau (Qgd) and switching losses. The non-linear capacitance simulations with variations in drain bias, including input (Ciss), output (Coss), and reverse transfer (Cgd/Crss) capacitances are shown in Fig. 6. An 80% improvement in Crss corresponds to the reduced gate-to-drain coupling with the deep p-base design, which induces an increased depletion width along the JFET region during the switching regime. Ciss and Coss remain the same for both devices as the remaining regions remain unaltered with a 5 µm cell pitch. Table 1 lists the performance metrics (BFOM, HF-FOM) and switching losses for both devices along with benchmarking results.

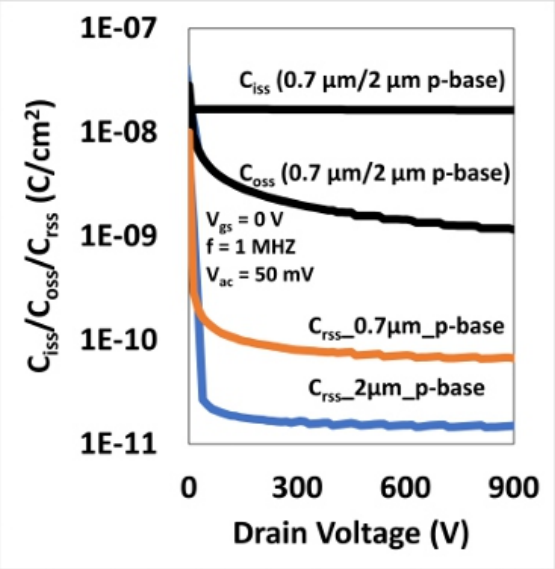

Fig. 6 Simulated non-linear input, output, and miller capacitances with drain bias with non-channeling 0.7 µm and channeling 2.0 µm p-base region in SiC MOSFETs.

Table 1 Simulated electrical performance metrics (BFOM and HF-FOM) at 27 °C and 150 °C.

0.7 µm p-base 1.2 kV 4H-SiC MOSFET				2.0 µm p-base 1.7 kV 4H-SiC MOSFET				Benchmark [Ref. 3]
T (°C)	BV (V)	$R_{on,sp}$ (mΩ-cm²)	BFOM (MV/cm²)	T (°C)	BV (V)	$R_{on,sp}$ (mΩ-cm²)	BFOM (MV/cm²)	Design parameters:
27	1208	2.4	608	27	1693	1.7	1686	W_{JFET} = 0.9 µm
150	1220	2.7	551	150	1700	2.0	1445	L_{ch} = 0.5 µm
	Q_{gd} (nC/cm²)	$R_{on,sp}$ (mΩ-cm²)	HF-FOM (nC-mΩ)		Q_{gd} (nC/cm²)	$R_{on,sp}$ (mΩ-cm²)	HF-FOM (nC-mΩ)	L_{drift} = 10 µm N_{drift} = 8×10¹⁵ cm⁻³
27	117	2.4	281	27	82	1.7	140	
150	117	2.7	433	150	82	2.0	164	Electrical parameters:
	E_{on} (mJ)	E_{off} (mJ)			E_{on} (mJ)	E_{off} (mJ)		$R_{on,sp}$ = 4 mΩ-cm² BV = 1560 V
27	2.1	0.8		27	1.7	0.8		

Conclusion

In this study, we showed that the single-step channeling implantation is a highly promising method for realizing high BFOM and low HF-FOM in 4H-SiC MOSFETs. In addition, the implementation of channeling implantation ensured a superior process throughput at a much lower cost than the standard multi-step implant process.

Acknowledgement

This work was supported by the Science and Engineering Research Council of A*STAR (Agency for Science, Technology and Research) Singapore, under Grant No. A20H9A0242.

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Economic Feasibility Analysis of Vertical High-Voltage 4H-SiC Superjunction MOSFETs Compared to Conventional Counterparts

Mohamed Torky1,a* and Woongje Sung1,b
1College of Nanotechnology Science and Engineering, University at Albany, Albany, NY 12203, USA

ABSTRACT

Vertical high-voltage 4H-SiC superjunction (SJ) MOSFETs have emerged as a superior alternative compared to conventional SiC MOSFET or Si IGBT, as SJ MOSFETs present a better trade-off between specific on-resistance (RON,sp) and breakdown voltage (BV). The fabrication of SJ devices requires precise, and multi-step processes, such as multi-epitaxial growth, trench-refill processes, and MeV implantations [3,4,5]. However, these methods increase the overall costs of SJ devices compared to their conventional counterparts, potentially undermining their benefits. This paper compares the chip costs of SJ and conventional MOSFETs at a wide range of BV and current ratings, evaluating the economic feasibility of SJ MOSFETs in 4H-SiC. Our results highlight the potential improvements in SJ fabrication and design to enhance cost-effectiveness, particularly for medium-voltage applications (>3.3kV).

Keywords: Cost Analysis, Economic Feasibility, SiC Superjunction MOSFETs, Fabrication

Introduction

In medium-voltage applications (>3.3kV), SiC MOSFETs (Fig. 1(a)) and Si IGBTs (Fig. 1(b)) are the main devices used. Despite their prevalence, these MOSFETs encounter issues such as high conduction losses in SiC MOSFETs due to the dominance of drift region resistance at these voltage ratings, and significant switching losses in Si IGBTs because of their bipolar nature. To address these challenges, vertical high-voltage 4H-SiC superjunction (SJ) MOSFETs (Fig. 1©) offer a better solution, enhancing both conduction and switching performance by reducing drift region resistance while maintaining a unipolar conduction. SJ devices provide a superior trade-off between specific onresistance (RON,sp) and breakdown voltage (BV) (RON,sp BV1.1) compared to the traditional, uniformly doped vertical power devices (RON,sp BV2.296), as illustrated in Fig. 2 [1]. However, the complex and expensive fabrication processes of SJ devices could limit their adoption over conventional devices. Therefore, estimating the costs of SJ and traditional devices is crucial to assess the advantages of superjunction devices at specific breakdown voltage and current ratings.

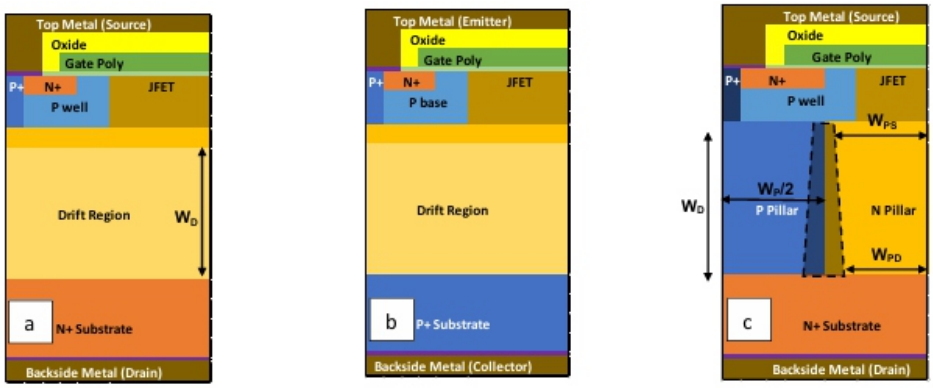

Fig.1. Schematic cross-section views of half unit cells of (a) conventional MOSFET, (b) IGBT and (c) SJ MOSFET.

Superjunction Theory

The key design of SJ devices is the alternating charge-balanced P and N pillars, where these pillars introduce a lateral electric field across their sidewalls to ensure a rectangular-like electric field profile along the vertical direction [2]. The lateral electric field is responsible for terminating the charges in the pillars laterally and deplete all the charges before breakdown occurs. Once the charges in the pillars are depleted laterally, the vertical electric field starts to develop uniformly. Only the thickness (WD) of the pillars imposes the breakdown voltage capability of the device [2]. As shown in Fig. 2, decreasing the pillar width decreases the specific on-resistance offsets by enhancing the doping of the pillars to keep the pillar charge dose the same(5um and 1 um lines).

Unlike conventional devices, ideally, the doping in the superjunction devices does not alter the effective critical electric field or the breakdown voltage providing that the dose is not higher than the optimal value and the charges in the pillars are balanced. Consequently, it is important to design the pillars width and doping to ensure the best trade-off between RON,sp and BV. Based on Gauss' law, the optimal pillar charge dose used here is 1013 cm-2 [2], ensuring an optimal RON,sp without breakdown at the sidewalls of the pillars. Moreover, the drift region thickness of superjunction devices is shorter than that of conventional devices at the same breakdown voltage due to the rectangular-like electric field profile, reducing the overall resistance even further. The fabrication of SJ devices necessitates precise processes involving multiple steps to ensure the desired charge-balanced pillars in terms of both doping and width, particularly for high voltage applications that require thicker pillars. Various techniques have been explored, including multiepitaxial growth [3], trench-refill processes [4], and a series of MeV implantations and epi-growth processes [5]. However, these methods contribute significantly to the overall cost of SJ devices, potentially outweighing their benefits compared to conventional devices with similar breakdown voltage and current ratings.

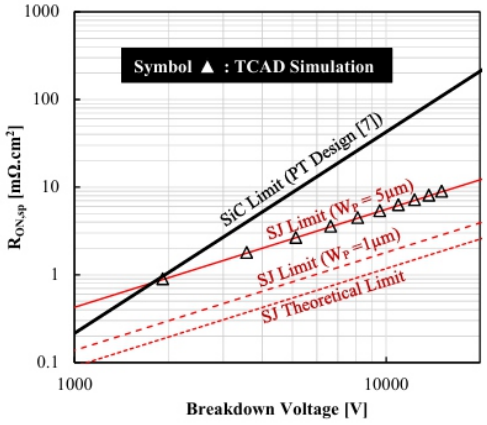

Fig.2. $R_{ON,sp}$ and breakdown voltage trade-off for conventional and superjunciton (SJ) devices with different SJ pillar widths.

Devices Modeling and Economic Analysis

We construct our cost model referring to GE's previous study [5], leveraging their scalable devices that exhibit less performance degradation. Instead of using multi-epitaxial growth or trenchrefill processes, a 12μm epitaxial growth followed by MeV ion-implantation fabrication cycle can be employed. This reduces overall costs and mitigates process variation when compared to other methods. According to [6], only one fabrication cycle can yield a 12μm charge-balanced pillars resulting in breakdown voltage >2kV. We used a closed form set to calculate the performance parameters as a function of drift layer thickness for conventional MOSFETs developed by [7] assuming a punch through (PT) design which exhibits the best RON,sp for a given BV compared to non-punch through (NPT) design. For SJ MOSFETs, we employed the simulation-based empirical formula developed by [8] for the blocking

performance (BV). While for the conduction performance, we have used the JFET depletion approximation of the alternating pillars [9] as shown in Table 1 where ρ is the resistivity of the pillars, WP is the pillar width, WD is the pillar vertical thickness, WPS is the pillar width at the source side and WPD is the pillar width at the drain side. The JFET depletion is assumed to be linear from the source to the drain where the voltage at the source is zero and the drain is 1V. Additionally, we validate our static calculations through 2D Sentaurus TCAD simulations.

Table 1. Conventional and Superjunction MOSFETs design parameters [7,8,9]

Parameters	Conventional MOSFETs	Superjunction MOSFET
N_D [cm^{-3}]	$8.839\times10^{19}\ BV^{-1.234}$ [7]	$10^{13}/W_P$ [9]
W_D [μm]	$2.625\times10^{-3}\ BV^{1.117}$ [7]	$2.15\times10^{-3}\ BV^{1.1}$ * [8]
$R_{ON,sp}$ [Ω.cm^2]	$2.791\times10^{-11}\ BV^{2.296}$ [7]	$\frac{W_P}{\rho(W_{PS}-W_{PD})} ln\left(\frac{W_{PS}}{W_{PD}}\right) W_D$ [9]

* Extracted and calculated from [8]

To estimate the active area for both MOSFETs, we have used Eq. (1), which is a thermal-based analysis according to the maximum power handling capability of the device [10],

$$Active\ Area = \sqrt{\frac{I^2 \times k \times R_{ON,sp\_300K} \times \left(\frac{T_{j,max}}{300}\right)^{\alpha}}{T_{j,max} - T_c}} \qquad (1)$$

where I is the current rating of the device, k is the specific thermal resistance assumed to be 0.068 K·cm^2/W, R_{ON,sp_300K} is the specific on-resistance at room temperature, α is temperature coefficient assumed to be 1.8, $T_{j,max}$ is the maximum junction temperature and T_c is the case temperature assumed to be 425K and 300K respectively. The model in Eq (1) has been plotted and matched with 1.2kV SiC commercial MOSFETs for different current ratings [10]. The chip size is calculated by assuming a periphery of 10μm which is the P+ ring around the edges of the active area and an edge termination (ET) width of 5 times the drift layer thickness (5×W_D) as depicted in Eq. (2).

$$Chip\ Size = \left(\sqrt{Active\ Area} + 2(10\mu m + 5 \times W_D)\right)^2 \qquad (2)$$

Since the active area is a function of $R_{ON,sp}$ with a square root dependence, and the edge termination width is a function of the drift region thickness, the total chip size is a function of BV as shown in Table 1. The active area is proportional to $\sqrt{R_{ON,sp}}$ which in turn is proportional to $\sqrt{BV^{2.296}}$ and $\sqrt{BV^{1.1}}$ for conventional and SJ MOSFETs respectively. Moreover, the edge termination width is a function of W_D which has the same BV dependence of $BV^{1.1}$ for both designs which means that the chip size due to the edge termination only has a dependence of $(BV^{1.1})^2$. For this reason, at lower BV where the active area dominates the total chip size, the active area of conventional MOSFETs is increasing with a higher rate than that of SJ MOSFETs. However, at a relatively higher BV where the edge termination of SJ starts to dominate the chip size, the chip size of SJ MOSFETs starts to increase by $(BV^{1.1})^2$ instead of $\sqrt{BV^{1.1}}$ increasing the rate of SJ chip density as depicted in Fig. 3. In this figure, SJ-to-conv. MOSFET chip density curve has an inflection point where the rate of increase of chip density starts to decrease. The SJ design in Fig. 3 has a pillar width of 5μm assuming 10A current rating.

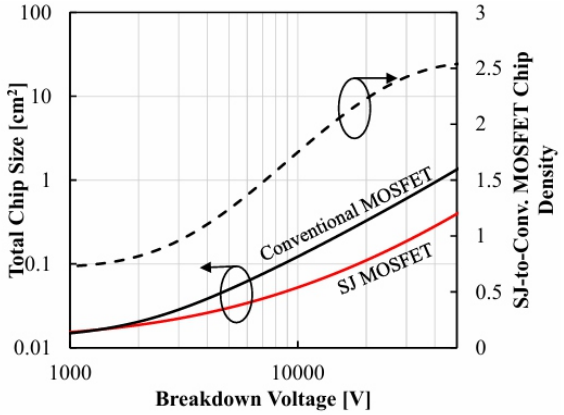

Fig. 3. Total chip size for conventional and superjunction MOSFET (left) and SJ-to-conventional MOSFET chip density assuming 10A current rating (right).

Based on the chip size of each MOSFET design, the price per chip is calculated using Eq. (3). For conventional MOSFETs, the substrate, epitaxial and fabrication costs are assumed to be $1000, a $50/µm and $1000, respectively. While SJ MOSFETs incur an additional cost of $500 and $2500 of an extra 12µm epi-growth operation and 12µm MeV ion implantation of both P and N pillars, respectively [4]. Table 2 illustrates all the cost and design assumption for both designs.

$$Chip\ Price = \left(\frac{Sub.cost + Epi.cost + Fab.cost}{\frac{Wafer\ size}{Chip\ size} \times Yield} \right) \times \frac{1}{Gross\ Margin} \quad (3)$$

Table 2. Cost Assumptions of Conventional and Superjunction MOSFETs

Assumptions	Conventional MOSFETs	Superjunction MOSFET
Substrate (Sub.) Cost	$1000	$1000
Epi Growth (Epi.) Cost	$50/$\mu$m	$50/$\mu$m + $500 per additional epi-growth
Fabrication (Fab.) Cost	$1000	$1000
MeV Ion Implant	NA	$2500 per run (12µm pillar) **(Variable)**
Wafer Size	6-inch	6-inch
Gross Margin	0.5	0.5
Yield	0.8	0.6 **(Variable)**
Pillar Width	NA	5 μm [4] **(Variable)**
Current Rating	10A **(Variable)**	10A **(Variable)**

Results and Discussion

We developed multiple cost scenarios and design approaches to evaluate the economic feasibility of 4H-SiC Superjunction (SJ) MOSFETs compared to conventional counterparts. The analysis covered three different fabrication cost scenarios (Cost #1, Cost #2, and Cost #3) and four chip design scenarios (Chip #1 to Chip #4) at varying breakdown voltage (BV) ratings, focusing on the points where SJ MOSFETs become more cost-effective than conventional MOSFETs as illustrated in Table 3 and 4.

SJ Cost Scenarios: The baseline cost (Cost #1) assumes a fabrication cost of $3000 for implementing

12µm charge-balanced pillars, while Cost #2 and Cost #3 explore reduced fabrication costs of $2000 and $1000 per 12µm pillar, respectively.

SJ Chip Scenarios: The design scenarios varied pillar width and manufacturing yield. Chip #1 served as the baseline, with a 5µm pillar width and 60% yield, while Chip #2 reduced the pillar width to 1µm. Chip #3 increased yield to 80%, and Chip #4 combined the narrower pillar width and higher yield for optimal performance.

Table 3. Different cost scenarios for SJ MOSFETs

Scenarios	MeV Ion Implant plus Epi overgrowth (12µm-thick Pillars) ($) [4]
SJ Cost #1	**$3000 ($2500 implant + $500 epi overgrowth)**
SJ Cost #2	**$2000**
SJ Cost #3	**$1000**

Table 4. Different chip design scenarios for SJ MOSFETs

Scenarios	Pillar Width, W_P (µm)	Manufacturing Yield for SJ MOSFET
SJ Chip #1	5	0.6
SJ Chip #2	**1**	0.6
SJ Chip #3	5	**0.8**
SJ Chip #4	**1**	**0.8**

As shown in Fig. 4, the chip price is plotted against the breakdown voltage for all chip and cost scenarios. The BV crossover is defined as the BV point where both conventional and SJ MOSFETs prices are even. In the Chip #1 scenario, the breakdown voltage crossover occurs at approximately 8.5 kV, assuming a fabrication cost of $1000 for each 12µm SJ drift region pillar (Cost #3). For Chip #2, reducing the pillar width to 1µm (the technological limit) significantly increases the chip density of SJ MOSFETs, as the specific on-resistance decreases by 50% compared to the 5µm width. This reduction leads to a 29% decrease in active area, with the BV crossover point dropping to kV, assuming the same $1000 fabrication cost, representing a 58% reduction in the crossover compared to Chip #1. In the Chip #3 scenario, where the yield is increased by 33% (from 0.6 to 0.8), the crossover occurs at approximately 2.3 kV and 20 kV, assuming $1000 and $2000 fabrication costs, respectively. This results in a 73% reduction in the BV crossover compared to Chip #1. For Chip #4, the crossover points are around 1.2 kV and 4.6 kV, assuming fabrication costs of $1000 and $2000, respectively, though there is no crossover with Cost #1. Table 5 summarizes the breakdown voltage crossovers for different chip and cost scenarios, assuming a 10A current rating.

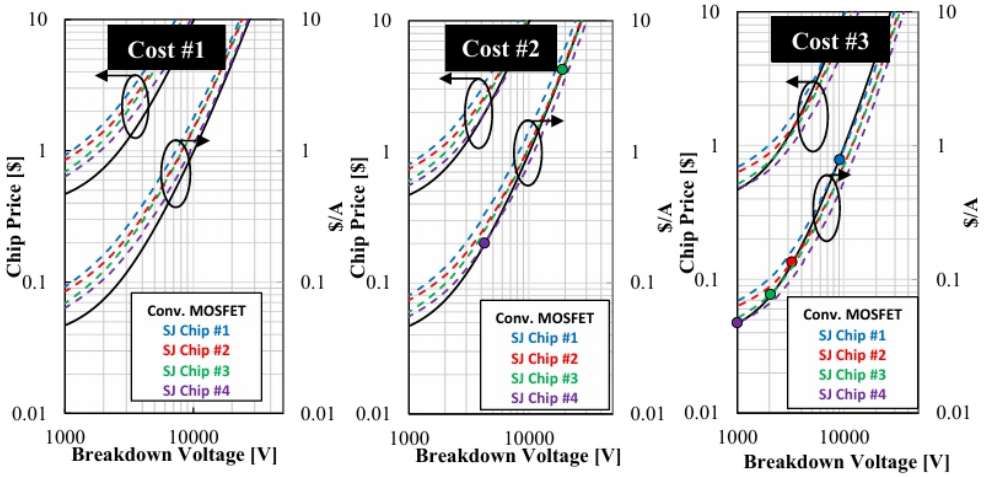

Fig. 4. Chip price and price per ampere for SJ MOSFETs with different design and cost scenarios compared to conventional MOSFETs assuming a current rating of 10A

Table 5. BV crossover and chip price per ampere for different SJ chip design and cost scenarios at 10A current rating.

Chip/Cost Scenarios (10A)	BV Crossover [kV]			Chip Price per Ampere [$/A]		
	Cost #1	Cost #2	Cost #3	Cost #1	Cost #2	Cost #3
SJ Chip #1	-	-	8.5	-	-	0.69
SJ Chip #2	-	-	3.6	-	-	0.15
SJ Chip #3	-	20	2.3	-	4.9	0.08
SJ Chip #4	-	4.6	1.2	-	0.22	0.05

Table 6. BV crossover and chip price per ampere for different SJ chip design and cost scenarios at 50A current rating.

Chip/Cost Scenarios (50A)	BV Crossover [kV]			Chip Price per Ampere [$/A]		
	Cost #1	Cost #2	Cost #3	Cost #1	Cost #2	Cost #3
SJ Chip #1	-	35	7.1	-	12.1	0.38
SJ Chip #2	34	9.2	3.5	11.2	0.64	0.12
SJ Chip #3	43	11	2.3	19.1	0.84	0.08
SJ Chip #4	9.3	3.9	1.2	0.65	0.14	0.05

Table 7. BV crossover and chip price per ampere for different SJ chip design and cost scenarios at 100A current rating.

Chip/Cost Scenarios (100A)	BV Crossover [kV]			Chip Price per Ampere [$/A]		
	Cost #1	Cost #2	Cost #3	Cost #1	Cost #2	Cost #3
SJ Chip #1	-	25	6.9	-	4.90	0.35
SJ Chip #2	20	8.6	3.4	3.09	0.52	0.12
SJ Chip #3	28	10	2.3	6.22	0.71	0.08
SJ Chip #4	8.7	3.9	1.2	0.54	0.14	0.05

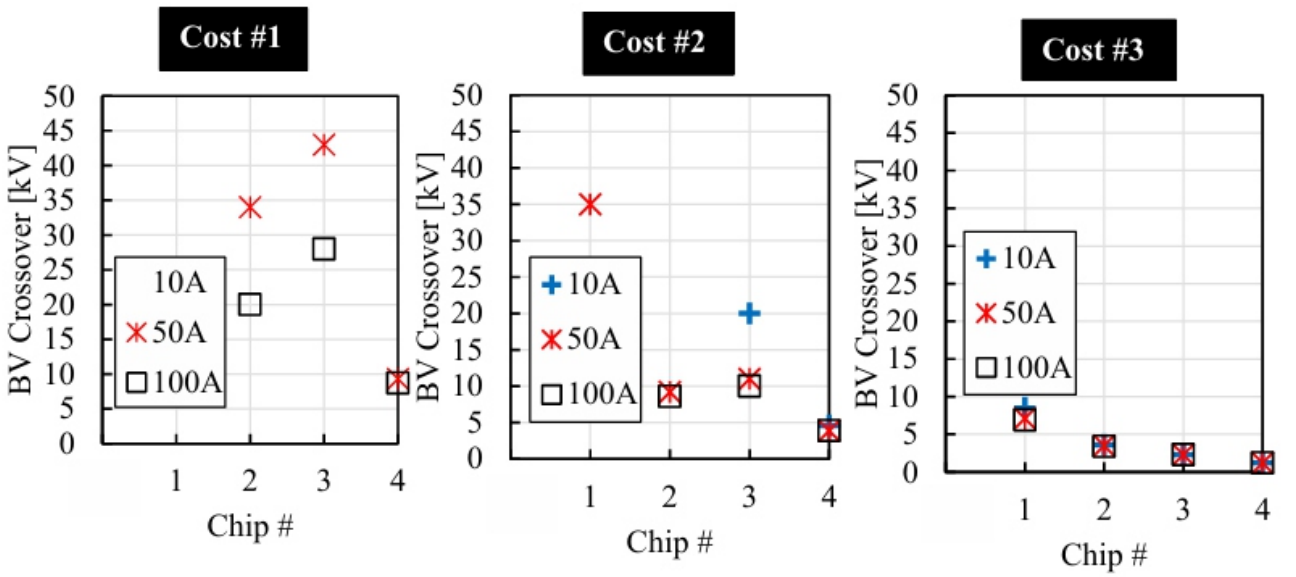

Fig. 5. BV crossover for all chip and cost scenarios at different current ratings. No data denotes no crossover.

At a 50A current rating as shown in Table 6, the breakdown voltage crossovers decrease across all chip scenarios at higher BV levels. This increase in SJ chip density is driven by the active area dominating the total chip size, rather than the edge termination. The dependence of the total chip size on the breakdown voltage is lower for SJ MOSFETs $\left(\sqrt{BV^{1.1}}\right)$ compared to conventional MOSFETs $\left(\sqrt{BV^{2.296}}\right)$ causing the crossover point to shift to the left, or decrease, at higher breakdown voltages. However, at lower BV values, the crossover point remains close to that of 10A, as the active area is already the dominant factor for both current ratings. While, at 100A current as shown in Table 7, the BV crossovers decrease for Cost #1 scenario even more as the active area is relatively more dominating compared to 50A current rating. Fig. 5 sums up all the BV crossovers for different chip and cost scenarios at 10A, 50A and 100A ratings.

Conclusion

The paper compares the economic feasibility of vertical high-voltage 4H-SiC Superjunction (SJ) MOSFETs with conventional SiC MOSFETs, focusing on the trade-off between specific onresistance (RON,sp) and breakdown voltage (BV). SJ devices offer superior performance, especially at higher voltages, by reducing drift region resistance and achieving a better RON,sp at a given BV. However, their complex fabrication processes significantly raise production costs. The analysis shows that despite the improved performance of SJ MOSFETs, their higher fabrication costs often limit their economic competitiveness compared to conventional MOSFETs, particularly at lower breakdown voltages and high-current applications. To make SJ MOSFETs economically feasible, the cost per chip must decrease or their yield and chip density must improve. The study concludes that SJ MOSFETs become more cost-effective as the breakdown voltage increases, especially in highvoltage and high-current applications, depending on the specific design and fabrication scenario. In summary, while SJ MOSFETs outperform conventional MOSFETs in high-voltage applications, reducing their production costs or improving fabrication processes is essential for widespread economic feasibility.

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