ISSN Application No. 21779

Journal of Wireless Communication and Simulation

Volume No. 12

Issue No. 1

May - August 2024

ENRICHED PUBLICATIONS PVT.LTD

JE - 18,Gupta Colony, Khirki Extn,
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Journal of Wireless Communication and Simulation

Aims and Scope

Journal of Wireless Communication and Simulation has become very important with the ever increasing demands of the software development to serve the millions of applications across various disciplines. For large software projects, innovative software development approaches are of vital importance. In order to gain higher software standards and efficiency, software process adaptation must be derived from social behavior, planning, strategy, intelligent computing, etc., based on various factors. This Journal addresses the state of the art of all aspects of software engineering, highlighting the all tools and techniques for the software development process.

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(Volume No. 12, Issue No. 2, May - August 2024)

Contents

Analysis of Bent Ground plane on MIMO Antenna

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A B S T R A C T

This paper presents the analysis of bent ground plane antennas for multiple-input-multiple-output (MIMO). Here, antenna array with three elements are proposed to evaluate the diversity performance of MIMO antennas systems. Then a three-element suspended plate antenna array with a bent ground plane is analyzed. The diversity performance of the design is analysed with the simulation results. At suspended angle α = 0o, the reflection coefficient of antenna is found to be - 26.58 dB with an isolation of -47.53dB at resonance frequency 5 GHz. While At suspended angle α = 45o, the reflection coefficient of antenna is found up to -29.69 dB with a maximum isolation of - 56.65dB.

Keywords – Correlation coefficient, diversity antenna, diversity gain, multiple-input multiple output (MIMO) antenna, phone antenna, total radiation power.

INTRODUCTION

Conventional Microstrip antenna consist a conducting patch printed on a grounded microwave substrate. It has the attractive features of light weight, small size, easy fabrication, low profile and conformable.

In this paper the performance evaluation of antennas in MIMO system is presented. After that, a three-element suspended plate antenna design with a bent ground plane is designed and analysed.The recent development of wireless technology has increased the capacity and reliability requirements of wireless communication systems. It is difficult to fulfil these requirements with traditional SISO (single-input single-output) systems, due to its limitations of less channel capacity. By using transmitting-diversity, diversity-reception, and channel-coding techniques, MIMO (multiple- input multiple-output) systems are able to transmit multiple signals, with the same power level, simultaneously through parallel channels. These signals are then received and combined using diversity techniques. MIMO becomes a popular technology due to its potential to achieve low bit error rate (BER) and larger capacity by multiplexing. MIMO multiplexing has been widely adopted due to its high speed data Communications [1-6].

Multiple-Input and Multiple-Output consists of multiple antennas at both the transmitter and receiver to

improve communication performance. One of the major benefits of MIMO systems over traditional SISO systems are their improved capacity and reliability, without increasing bandwidth or transmitted power.

In a MIMO system, the antennas have a great impact on the channel capacity, also it plays an important role in system stability. Antenna arrays used in MIMO systems are required to have high gain, wide lobe pattern, and high isolations between antenna elements. Now, the performance of MIMO antenna is degraded due to mutual coupling between elements. There are different strategies have been devised to achieve decoupling (or improve isolation) among the antennas[2,5].

The RF performance of antennas are evaluated by using various parameters such as gain, directivity, radiation patterns, matching impedance, and polarization, the envelope correlation coefficient between antennas. The envelope correlation coefficient calculated using S-parameters or radiated electric fields with assumption that the antennas are lossless and the channels are uniform and random [4].

Using the S-parameters of N elements, the envelope correlation coefficient, ρe,ij can be given in equation1.1:

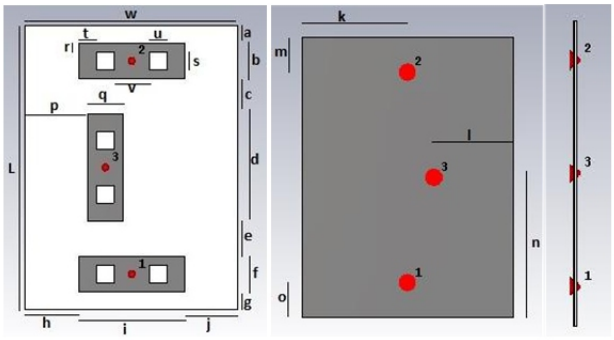
$$\rho_{-}(i,j,N) = \frac{\left|\sum_{n=1}^{N} S_{i,n}^{*} S_{n,j}\right|^{2}}{\prod_{k=i,j}\left|1-\sum_{n=1}^{N} S_{k,n}^{*} S_{n,k}\right|} \quad \text{---------1.1}$$

Where, i and j indicate the i^{th} and j^{th} elements, respectively. It can be observed that the correlation is affected by the inter-element mutual coupling, the phase difference between S_{ii} and S_{ij} and impedance matching. From the denominator term it can be observed that S_{ii} and S_{ij} also affect the overall radiated power from all the elements. As a result, both factors affect the antenna efficiency. The variation in the envelope correlation coefficient is caused by the phase change in the numerator term [4, 6].

Design And Simulation

A. MIMO antenna with $\alpha = 0^0$

The optimized design with dimensional details of the proposed MIMO antenna is illustrated in Fig. 1.The dimensions are in millimetre (mm): W=120, L=160, a=10, b=20, c=20, d=60, e=20, f=20, g=10, h=30, i=60, j=30, p=35, q=20, r=5, s=10, t=10, u=10, v=30, k=60, l=45, m=20, n=80, o=20.The thickness of substrate is 1.6mm. A dielectric constant was 4.3. The overall size of MIMO antenna system is $120\times160\times 1.6mm^3$.



(a) Top layer (b) Bottom layer (c) side view

Fig. 1. Geometry of the MIMO antenna system α=0°

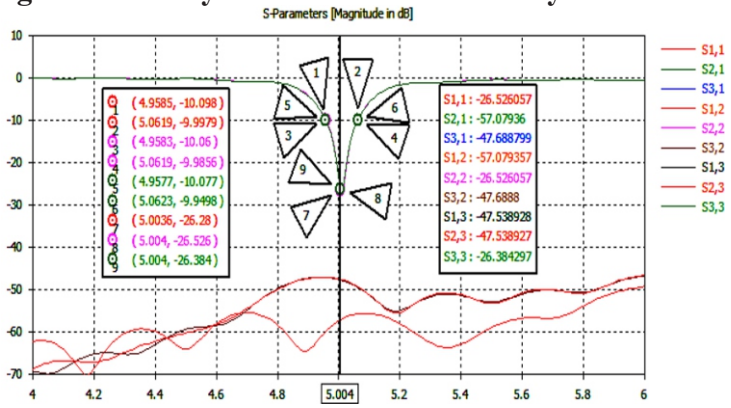
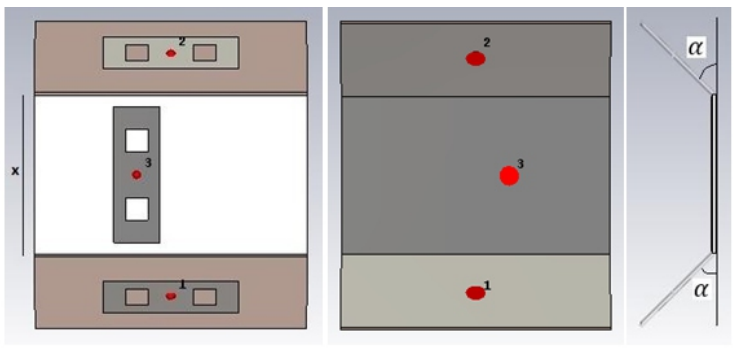


Fig.2 Simulated S-parameter with α =0°

After simulation, one frequency band is observed i.e. 4.95-5.06GHz with resonant frequency 5GHz. The reflection coefficient (S11) observed at 5GHz is -26.38dB with isolation varies between - 47.53dB to -57.09dB as shown in fig 2.The VSWR is 1.09 at 5 GHz. The gain observed at 5 GHz is 2.84dBi

B. MIMO antenna with α = 45°

In iteration2, the portions of the ground plane are bent i.e α = 45^0 as shown in figure 3, the mutual coupling between Elements 1 and 2 is found to be reduced such that the lowest coupling is achieved. The similar trend is also demonstrated for Elements 1 and 3. However, the mutual coupling between Elements 2 and 3 is also reduced. The value of correlation coefficient can be significantly reduced between Elements 1 and 2 as well as Elements 1 and 3 when α=45^0.



(a) Top layer (b) Bottom Layer (c) side view

Fig.3 Geometry of MIMO antenna with α=45°

The α = 450 gives one frequency band observed between 4.94-5.04 GHz with resonant frequency of 5GHz, The value reflection coefficients (S11, S22, S33) at 5GHz are found up to - 29.67dB is shown in fig.4. After introducing α = 450 , and the transmission coefficients are change in the range of -48.56 dB to -58.65dB which indicate the good isolation between elements. The VSWR is 1.06 at 5 GHz. The gain observed at 5GHz operating frequency is 1.03dBi.

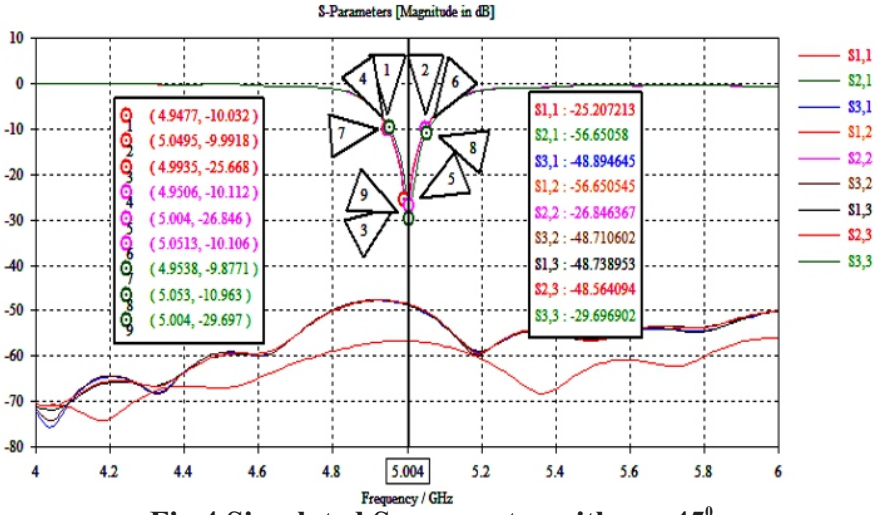


Fig.4 Simulated S-parameter with α = 45^0

C. MIMO antenna with α = 60^o

In iteration 3, the portions of the ground plane are bent i.e α = 60^0 as shown in figure 5. The correlation is significantly reduced between Elements 1 and 2 as well as Elements 1 and 3 when α=60^0. The value of correlation coefficient is found below 0.0002 in both cases.

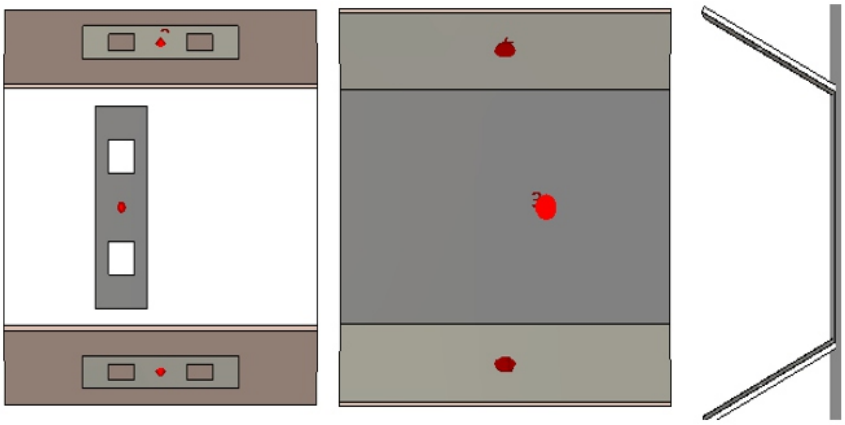


Fig.5 Geometry of MIMO antenna with α=60^o

The **α** = 60^0 gives one frequency band observed between 4.91-5.01 GHz with resonant frequency of 4.96GHz but resonance frequency of element 3 is shifted to 5 GHz. The value reflection coefficients (S11, S22, S33) are range between -26.94dB to -28.27 dB as shown in fig.4. After introducing **α** = 60^0 , and the transmission coefficient found in the range of -50.50 dB to -58.46 dB which indicate the good isolation between elements. The VSWR is observed below 2 at 5 GHz. The gain observed at 5GHz operating frequency is 1.87dBi.

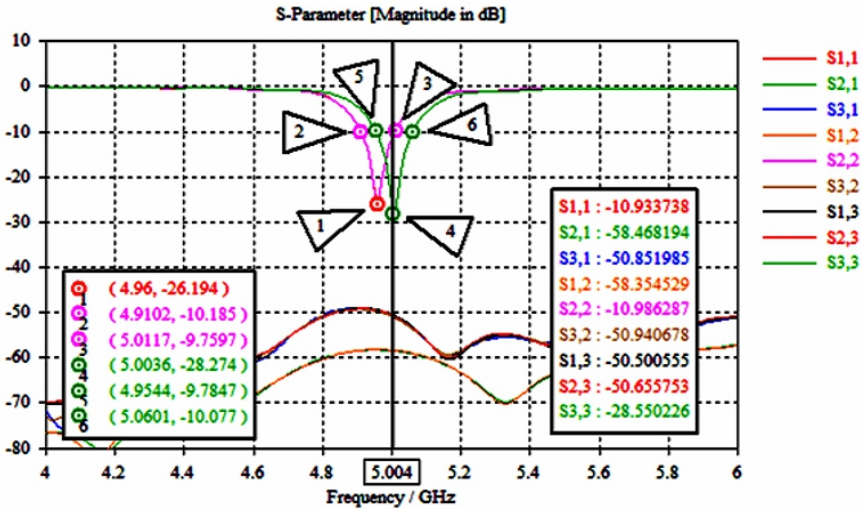


Fig.6 Simulated S-parameter with α = 60°

D. MIMO antenna with α = 90°

In iteration 4, the portions of the ground plane are bent i.e α = 90° as shown in figure 7, the mutual coupling between Elements 1 and 2 is found to be reduced such that the lowest coupling is achieved. The similar trend is also demonstrated for Elements 1 and 3. However, the mutual coupling between Elements 2 and 3 is also reduced. The correlation can be significantly reduced between Elements 1 and 2 as well as Elements 1 and 3 when α=90°.

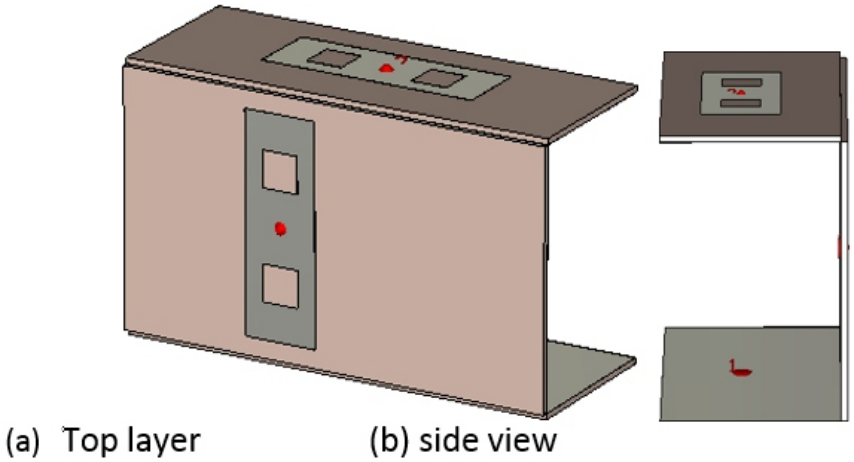


Fig.7 Geometry of MIMO antenna with α=90°

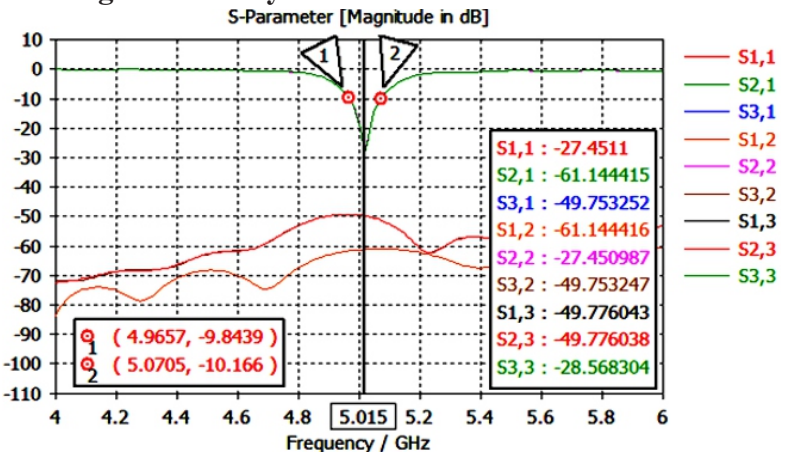
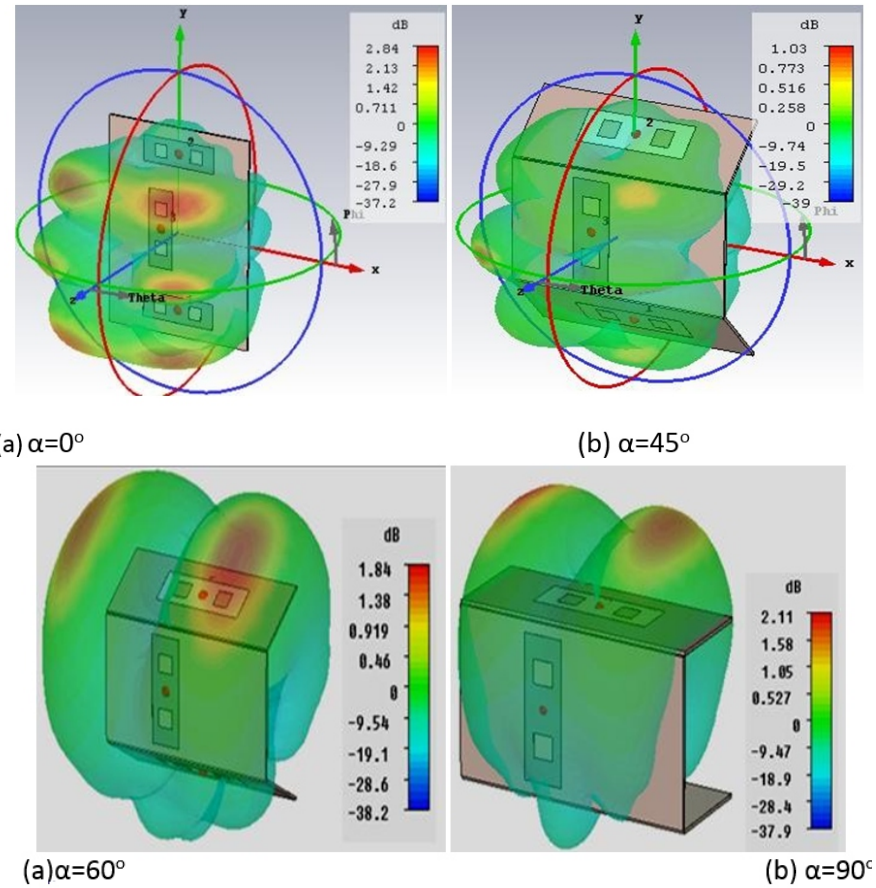


Fig.8 Simulated S-parameter with α = 90°

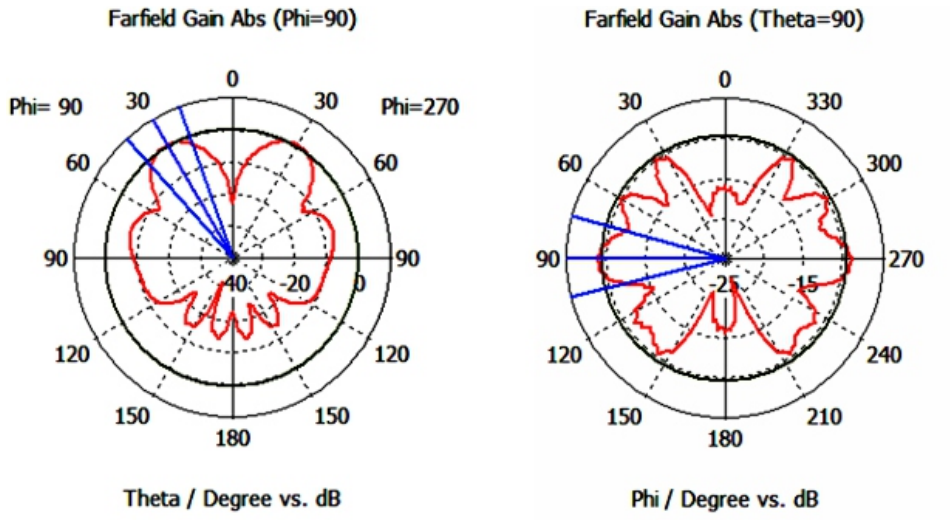
The $\alpha = 90^0$ gives one frequency band observed between 4.96-5.07 GHz with resonant frequency of 5 GHz. The value reflection coefficients (S11, S22, S33) are range between -27.94dB to -28.56dB as shown in fig.8. After introducing $\alpha = 60^0$, and the transmission coefficient found in the range of -50.50 dB to -58.46 dB which indicate the good isolation between elements. The VSWR is observed 1.08 at 5 GHz. The gain of antenna at 5GHz operating frequency is found up to 2.09dBi. The value of correlation coefficient is found below 0.00006.



(a) α=0° (b) α=45°

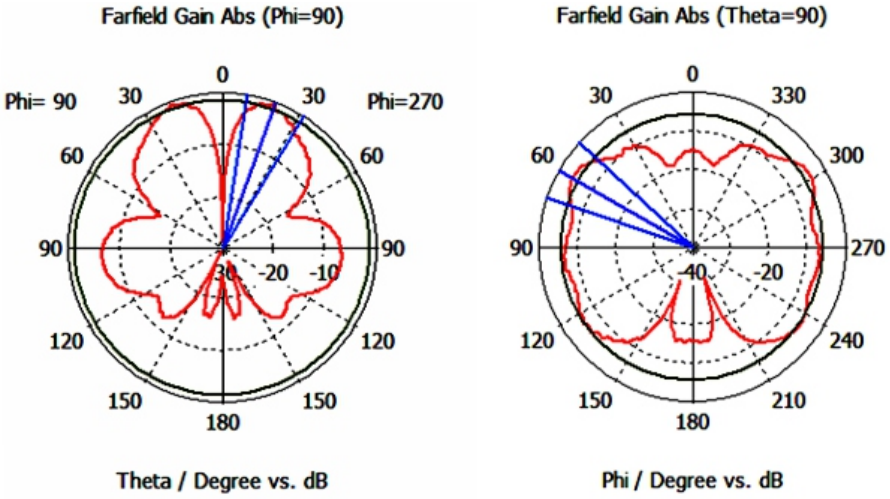
(a)α=60° (b) α=90°

Fig.9 Simulated 3D gain



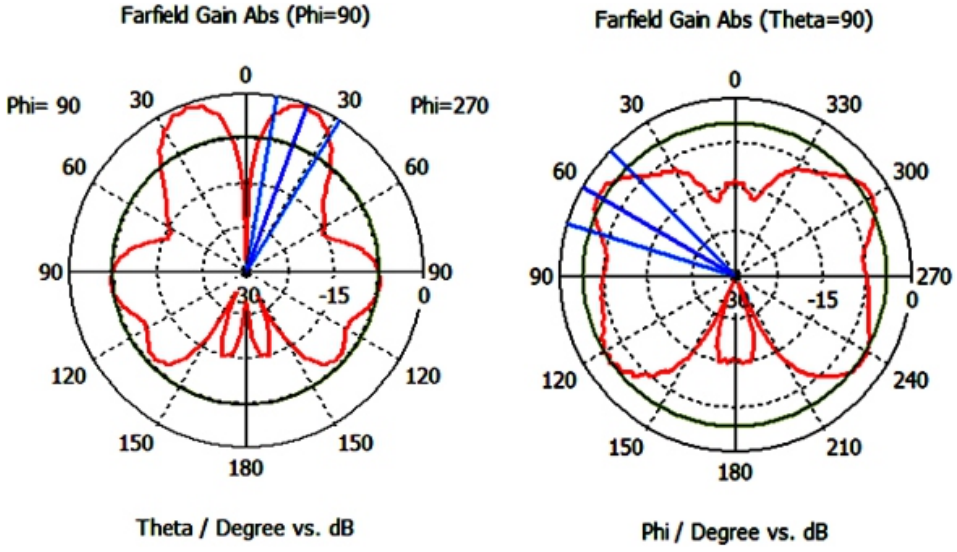
(a) Vertical far field gain (b) Horizontal far field gain

Fig.10 2D gain with α=0°



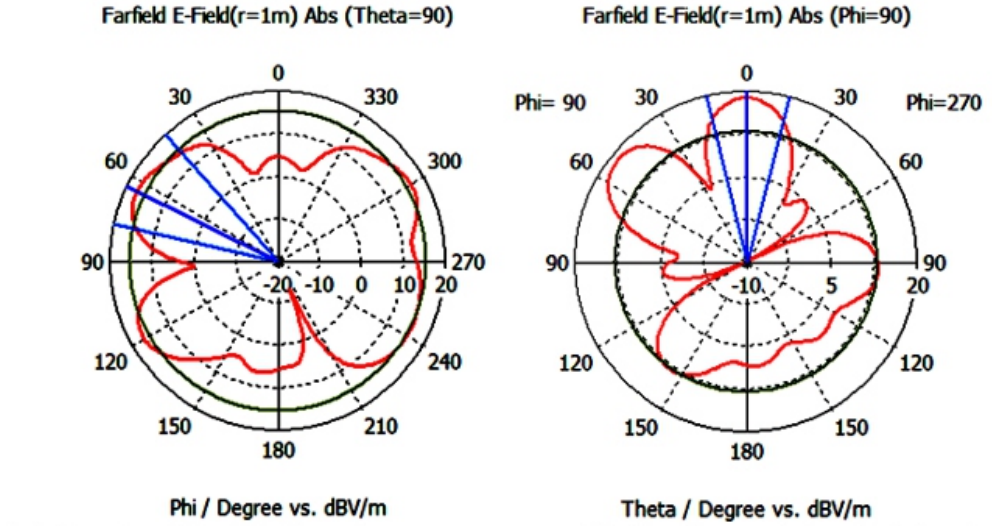
(a) Vertical far field gain (b) Horizontal far field gain

Fig.11 2D gain with α=45°



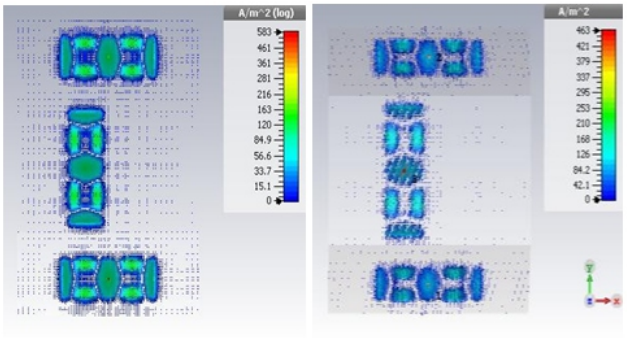
(a) Vertical far field gain (b) Horizontal far field gain

Fig.12 2D gain with α=60°

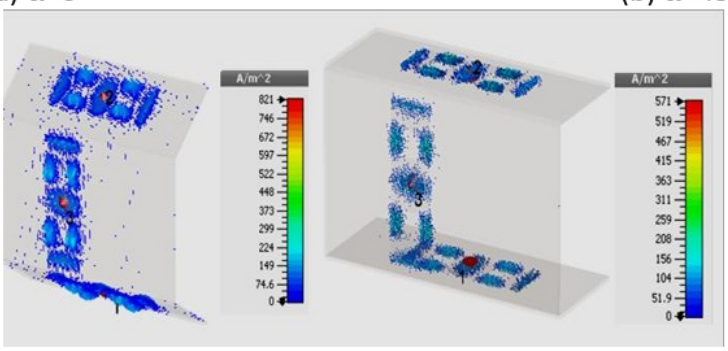


(a) Vertical far field gain (b) Horizontal far field gain

Fig.13 2D gain with α=90°



(a) α=0° (b) α=45°



(c) α=60° (d) α=90°

Fig.14 Current distribution of MIMO antenna

RESULTS AND DISCUSSIONS

From above diagram it is found that the results are link with mutual coupling factor. For better result, we fixed some parameters like feed position, dielectric constant, height of dielectric, patch size at optimum level. By changing the angle of ground plane further analysis can be done. Figure 9 shows 3D radiation pattern of MIMO antenna with and without bending the ground plane.

First, we simulate antenna system without bending ground plane i.e. α = 00 and It is observed that the structure hardly affects the impedance matching. Also check the effect of mutual coupling between antenna elements at resonance frequency 5 Ghz.

In iteration 2, the portions of the ground plane are bent i.e. α = 450 as shown in figure 3, the mutual coupling between Elements is found to be reduced such that the lowest coupling is achieved. The correlation can be significantly reduced between Elements 1 and 2 as well as Elements 1 and 3 when $\alpha=45^0$.

In iteration 3, the portions of the ground plane are bent by $\alpha = 60^0$ as shown in figure 5. The correlation can be significantly reduced below 0.0002 between Elements 1 and 2 as well as Elements 1 and 3 when $\alpha=60^0$.

In iteration 4, the portions of the ground plane are bent by $\alpha = 90^0$ as shown in figure 7. The correlation

can be significantly reduced below 0.00006 between Elements 1 and 2 as well as Elements 1 and 3 when $\alpha=90^0$. Also the gain achieved by antenna is above 2dBi.

CONCLUSION

Antenna array with 1.6 mm thick FR4 substrate is investigated in this paper. The analysis of bent plane with angle $\alpha= 0^0,45^0,60^0,90^0$ is carried out. Besides the conventional assessment of performance of MIMO antennas, the two- and three-dimensional patterns for envelope correlation coefficients have been proposed to evaluate the performance of the antenna designs. It has been found that for the given ground plane size and antenna configuration, the three-element antenna array on the 90o bent ground plane give better isolation than others. While the gain of antenna is found above 2 dBi for 00& 900. The results show that the proposed antenna can be used for wireless internet access application, which include WLAN. Here multipath fading avoid by providing spatial and pattern diversity.

REFERENCES

[1] Abouda , H.M.E1-Sallabi, and S.G.H "Aggman," Effect of Antenna Array Geometry And Ula Azimuthal Orientation on MIMO channel Properties In Urban City Street Grid, Progress In Electromagnetic Research, Pier 64, 257-278, 2006

[2] B. K. Lau and Z. Ying, "Antenna design challenges and solutions for compact MIMO terminals," in Proc. Int. Workshop Antenna Technol.(IWAT'2011)

[3] Chua Hai Yeow Eugene, Kei Sakaguchi, Hidekazu Murata, Kiyomichi Araki, "MIMO Array Antenna Design Criterion"

[4] Dr,Jacob Sharony, "Introduction To Wireless MIMO –Theory and Application," IEEELi, November 15, 2006

[5] Fitri Yuli Zulki And Eko Tjipto Rahardjo, "Compact MIMO Microstrip Antenna with Defected Ground For Mutual Coupling Suppression", Progress In Electromagnetics Research Symposium Proceedings, Marrakesh, Morocco, Mar.23,2011

[6] Zhi Ning Chen, Fellow, IEEE, Xue Ni Low, and Terence S.P.See, "Analysis and Optimization of Compact Suspended Plate MIMO Antennas," IEEE Antenna Propag.,vol, 59,No.1, JANUARY 2011.

Improved Continuous Neighbors Discovery Protocol for Wireless Sensor Networks

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ABSTRACT

A sensor network may contain a huge number of simple sensor nodes that are deployed at some inspected site. In large areas, such a network usually has a mesh structure .In most sensor networks the nodes are static. Nevertheless, node connectivity is subject to changes because of disruptions in wireless communication, transmission power changes, or loss of synchronization between neighboring nodes. Hence, even after a sensor is aware of its immediate neighbors, it must continuously maintain its view, a process we call continuous neighbor discovery. In this we discuss about the solution to the more power consumption during the neighbors discovery in wireless sensor network. Each sensor coordinate effort to reduce power consumption without increasing the time required to detect hidden sensors.

Keywords – neighbor discovery , wireless sensor network component.

INTRODUCTION

Despite the static nature of the sensor nodes, after the network has been established its connectivity is still subject to changes. In particular, even after a sensor node is aware of its immediate neighbors, it must continuously look for new ones in order to accommodate the following situations:

1. Loss of local synchronization due to accumulated clock drifts.
2. Disruption of wireless connectivity between adjacent nodes by a temporary event, such as a passing car or animal, a dust storm, rain or fog. When these effects disappear, the hidden nodes must be rediscovered.
3. The ongoing addition of new nodes, in some networks to compensate for nodes which have ceased to function because their energy has been exhausted (so-called dead nodes).
4. The increase in transmission power of some nodes, in some networks, in response to certain events, such as loss of connectivity with neighboring nodes or detection of important local happening.

For these reasons, detecting new links and nodes in sensor networks must be considered as an ongoing process. In the following discussion we distinguish between the detection of new links and nodes during initialization and their detection during normal operation. The former will be referred to as initial neighbor discovery whereas the latter will be referred to as continuous neighbor discovery. While previous works [8, 3, 5] address initial neighbor discovery and continuous neighbor discovery as similar tasks, to be performed by the same protocol, we claim that they should be addressed by different protocols for the following reasons:

- Initial neighbor discovery is usually performed when the sensor has no clue about the structure of its immediate surroundings. In particular, the sensor cannot communicate with the gateway, and is therefore very limited in performing its tasks. Hence, in this state for the sake of quicker detection, more extensive energy use is justified. It is very important to detect the immediate surroundings as soon as possible in order to establish a path to the gateway and to contribute to the operation of the network. In contrast, continuous neighbor discovery is performed when the sensor is already operational. This is a long-term process whose optimization is crucial for increasing the network life time.

- When the sensor performs continuous neighbor discovery, it is already aware of most of its immediate neighbors. It can therefore perform continuous neighbor discovery together with these neighbors in order to consume less energy. In contrast, initial neighbor discovery is an individual task, that must be executed by each sensor separately.

We now show, by means of an example, why an initial neighbor discovery protocol is inefficient for continuous neighbor discovery. Figure 1 presents a simple protocol. In this figure we assume that node u is in the initial neighbor discovery state, where its main task is to search for new neighbors. To this end, it periodically wakes up, at random times, and transmits a bunch of HELLO messages (the bunch size in the figure is 1). In the figure we see that the first 5 bunches of HELLO messages are transmitted when node v is sleeping, and therefore they cannot be received by v. The 6th bunch is transmitted when v is in active mode. Therefore, v is likely to receive at least one message of the 6th bunch, to which it responds with HELLO-ACK. From this time, the two nodes view each other as neighbors, and they maintain this relationship using periodic HELLO messages.

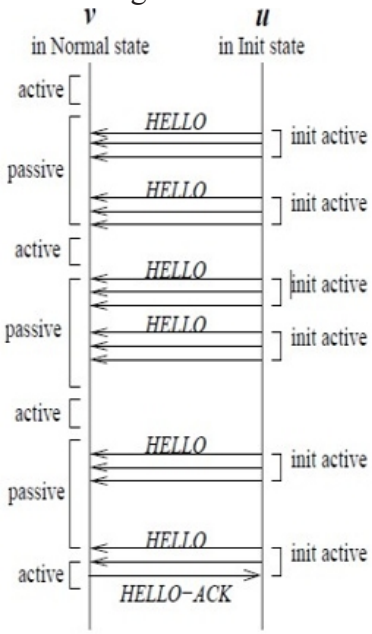

Figure 1: The transmission of HELLO control messages during neighbor discovery state

If a hidden node has duty cycle of 1%, we can assume that the discovering node v "hits" u when u is awake with probability of 1%. In this case, by the rules of geometric distribution, the discovery demands, in average, 100 bunches of HELLO messages. Hence, in order to guarantee the average discovery time of 10 seconds, u has to wake up every 0.1 second. Even if every wakeup lasts only 10msec, it gives us the duty cycle of 10 %, thereby expending a lot of its energy on finding its neighbors. Working with such a duty cycle might be reasonable only when node u is added to thenetwork, i.e., in the neighbor discovery state, but not as an ongoing algorithm for continuous neighbor discovery.

We distinguish between initial and continuous neighbor discovery in sensor network. Figure 5.2 summarizes this idea. When node u is initialized, it performs initial neighbor discovery. After a certain time period in the initial neighbor discovery state, during which the node is expected, with high probability, to find most of its neighbors, the node moves to the continuous neighbor discovery state. The main idea behind the continuous neighbor discovery scheme proposed in this chapter is that the task of finding a new node is divided among all the nodes in its vicinity.

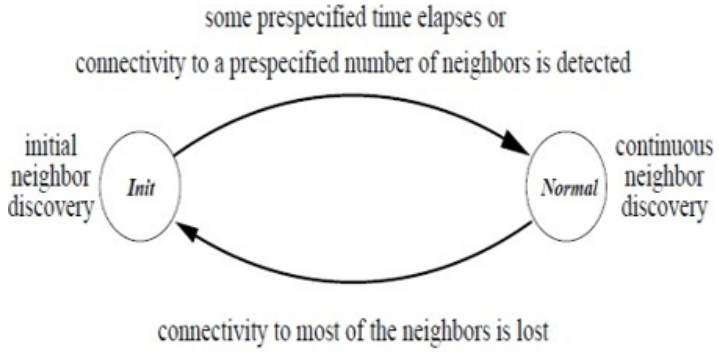

Figure 1.2: Continuous Neighbor Discovery vs. Initial Neighbor Discovery in Sensor Networks

II. BASIC SCHEMES AND PROBLEM DEFINITION

In the following discussion, two nodes are said to be neighboring nodes if they have direct wireless connectivity. We assume that all nodes have the same transmission range, which means that connectivity is always bidirectional. For our analysis we also assume that the network is a unit disk graph; namely, any pair of nodes that are within the transmission range of each other are neighboring nodes. Two nodes are said to be directly connected if they have discovered each other and they are aware of the wake up times of each other. Two nodes are said to be connected, if there is a path of directly connected nodes between them. A set of connected nodes is referred to as a segment. Consider a pair of neighboring nodes that belong to the same segment but are not aware that they have direct wireless connectivity. See, for example, nodes a and c in Figure 2(a). These two nodes can learn about their hidden wireless link using the following simple scheme.

Scheme 1 (detecting a hidden link inside a segment) One of the segment nodes issues a special SYNC

message to all segment members, asking them to wake up and periodically broadcast abunch of HELLO messages. This SYNC message is distributed over the already known wireless links of the segment. Thus, it is guaranteed to be received by every node in the segment. By having all the nodes wake up "almost at the same time" for a short period, we can ensure that all the wireless links between the segment's members will be detected with minimum energy cost.

This scheme needs to be involved only when a new node is discovered by one of the segment nodes. The discovering node will also be the node, that triggers the protocol.

suppose that every node wakes up once a second in order to receive messages from its in- segment neighbors. Suppose also that the node stays active for about 10 milliseconds, thereby having a duty cycle of 0.1%. In this case, the SYNC message can reach every node in the segment within at most D seconds, where D is the distance between the segment leader and the farthest node. The SYNC message carries a WAKE-UP-TIME field, which is initialized to D and decremented by t(v;u) by every node v that transmits the SYNC, where t(v;u) is the interval between the time v receives the SYNC and the time it transmits it to its in-segment neighbor u. Since this scheme is not frequently involved, we can allow nodes to remain active for a relatively long period of time, compensating for possible synchronization inaccuracy.

Scheme 2 (detecting a hidden link outside a segment) Node u wakes up randomly, every T(u) seconds on the average, for a fixed period of time H. During this time it broadcasts several HELLO messages, and listens for possible HELLO-ACK messages sent by new neighbors. The value of T(u) is as follows:

- T(u) = TI , if node u is in the initial neighbor discovery state of Figure 2.
- T(u) = TN(u), if node u is in the continuous neighbor discovery state of Figure 2, where TN(u) is computed according to the scheme presented in Section 4.

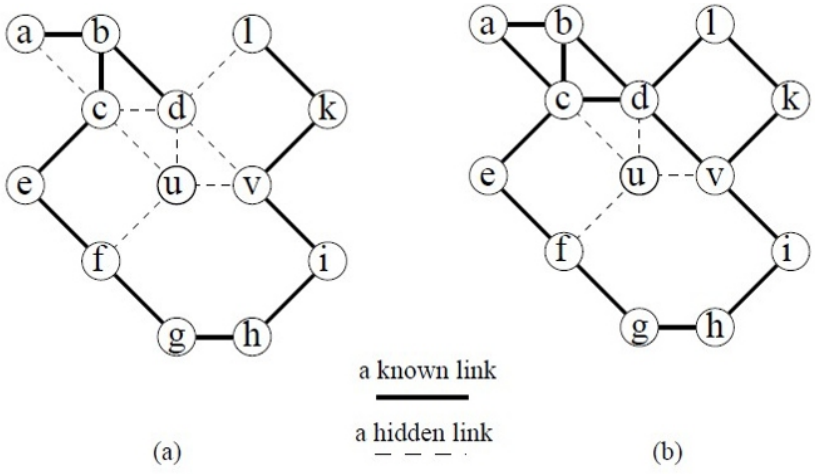

Figure 2: Segments with Hidden Nodes and Links

By Scheme 1, the discovery of an individual node by any node in a segment leads to the discovery of this node by all of its neighbors that are part of this segment. Therefore, discovering a node that is not yet in the segment can be considered a joint task of all the neighbors of this node in the segment. As an example, consider Figure 2(a), which shows a segment S and a hidden node u. In this figure, a dashed line indicates a hidden wireless link, namely, a link between two nodes that have not yet discovered each other. A thick solid line indicates a known wireless link. After execution of Scheme 1, all hidden links in S are detected (see Figure 2(b)). The links connecting nodes in S to u are not detected because u does not belong to the segment. Node u has 4 hidden links to nodes in S. Hence, we say that the degree of u in S is degS (u) = 4. When u is discovered by one of its four neighbors in S, it will also be discovered by the rest of its neighbors in S as soon as Scheme 1 is re-invoked. Consider one of the four segment members that are within range of u, node v say. Although it may know about the segment members within its own transmission range, it does not know how many segment neighbors participate in discovering u.

III. PROPOSED SYSTEM

For detecting new links and nodes in sensor networks must be considered as an ongoing process. In the following discussion we distinguish between the detection of new links and nodes during initialization, i.e., when the node is in Init state, and their detection during normal operation, when the node is in Normal state. The former will be referred to as initial neighbour discovery whereas the latter will be referred to as continuous neighbour discovery. Whileprevious works [1], [2], [3] address initial neighbour discovery and continuous neighbour discovery as similar tasks, to be performed by the same scheme, we claim that different schemes are required

A. Estimating The In-segment Degree of A Hidden Neighbor

we consider the discovery of hidden neighbors as a common task to be performed by all segment nodes. To determine the discovery load to be imposed on every segment node, we need to estimate the number of in-segment nodes that are neighbors of every hidden node. That is the in-segment degree of the hidden neighbor, denoted by degS(u). In this section we present methods that allow node v in the continuous neighbor discovery state to estimate the number degS (u) of in-segment neighbors of its hidden neighbor u. Node u is assumed not to be connected to the segment yet, and it is in the initial neighbor discovery state. Three methods are presented:

- Node v measures the average in-segment degree of the segment's nodes, and uses this number as an estimate of the in-segment degree of u. The average in-segment degree of the segment's nodes can be calculated by the segment leader. To this end, it gets from every node in the segment a message indicating the in-segment degree of the sending node, which is known due to Scheme 1. We assume that the segment size is big enough for the received value to be considered equal to the expected number of neighbors of every node.

- Node v discovers, using Scheme 1, the number of its in-segment neighbors, degS(v), and views this number as an estimate of degS(u). This approach is expected to yield better results than the previous one when the degrees of neighboring nodes are strongly correlated.
- Node v uses the average in-segment degree of its segment's nodes and its own in-segment degree degS(v) to estimate the number of node u's neighbors. This approach is expected to yield the best results if the correlation between the in-segment degrees of neighboring nodes is known. A special case is when the in-segment nodes are uniformly distributed.

The in-segment degree of v and u depends on how the various nodes are distributed in the network. Let X be a random variable that indicates the degree degS(v) of v in the segment S. Let Y be a random variable that indicates the degree degS (u) of u in S. Note that u itself is not aware of the value of Y . Let Y' be the value of Y estimated by v. Clearly, we want Y' to be as close as possible to Y . In what follows we analyze the three methods considered above and compare their accuracy and applicability. Since the in-segment degree of both the segment node (v) and the non-segment node (u) may have different values for different segment nodes, we use the mean square error measure (MSE) to decide how good the estimate is. The MSE is defined as E((Y- Y')2). Since v and u are two random nodes in the same graph, we can claim that X andY have the same distribution. Let us denote the correlation between X and Y , corr(X; Y), by C.

We assume that the node's average degree is small compared to the network size.
Let us denote the average graph degree by μ Clearly, E(X) = E(Y) = μ for the first method, the following holds:

$$MSE1 = E((Y- Y')^2) = E((Y - \mu)^2$$
$$= \mathrm{Var}(Y)$$

For the second method, we have $Y'= X$. Hence,

$$MSE2 = E((Y- Y')^2) = E((Y- X)^2)$$

$$\begin{aligned} MSE_2 &= E((Y-Y')^2) = E((Y-X)^2) \\ &= \sum_x \sum_y (y-x)^2 P(X=x, Y=y) \\ &= \sum_x \sum_y (y^2 - 2xy + x^2) P(X=x, Y=y) \\ &= E(X^2) + E(Y^2) - 2E(XY). \end{aligned}$$

$$MSE2 = E(X^2) + E(Y^2) - 2(C\ \mathrm{Var}(X) + E(X)E(Y))$$
$$= E(X^2) + E(X^2) - 2C\ \mathrm{Var}(X) - 2E(X)E(X)$$
$$= 2E(X^2) - 2E(X)^2 - 2C\ \mathrm{Var}(X)$$
$$= 2\mathrm{Var}(X) - 2C\ \mathrm{Var}(X)$$
$$= (2 - 2C)\mathrm{Var}(X)$$

for third method

$$MSE3 = E((Y' - Y)^2)$$

$$= E((CX + (1 - C)\,\mu - Y)^2)$$

$$= E(C^2 X^2 + 2C(1 - C)X\,\mu - 2CXY - 2(1 - C)\,\mu\, Y + (1 - C)^2\,\mu^2 + Y2)$$

$$= C^2\,E(X^2) + 2C(1 - C)E(X)\,\mu - 2CE(XY) - 2(1 - C)\,\mu\,E(Y) + (1 - C)^2\,\mu + E(Y^2)$$

$$= C^2\,E(X^2) + E(Y^2) + (2C - C^2 - 1)\,\mu^2 - 2CE(XY).$$

Using the fact that X and Y have the same distribution.

$$\begin{aligned} MSE_3 &= (C^2+1)E(X^2) + (2C - C^2 - 1)\mu^2 \\ &\quad -2C(C\,\mathrm{Var}(X) + \mu^2) \\ &= (C^2+1)E(X^2) - (C^2+1)\mu^2 - 2C^2\,\mathrm{Var}(X) \\ &= (C^2+1)(E(X^2) - \mu^2) - 2C^2\,\mathrm{Var}(X) \\ &= (C^2+1)\,\mathrm{Var}(X) - 2C^2\,\mathrm{Var}(X) \\ &= (1 - C^2)\,\mathrm{Var}(X) \end{aligned}$$

Hence, we have the following accuracy for the three estimation approaches:

1. Var(X)
2. (2 - 2C)Var(X)
3. (1 – C^2)Var(X)

Let u, v and w be nodes in a geometric graph with the same transmission range, where nodes are distributed uniformly. If u is a neighbor of v and v is a neighbor of w, then the probability that u is also a neighbor of w is $P=1 - \frac{3}{4\pi}\sqrt{3} = 0.586503$.

if we assume uniform distribution of nodes, the three estimation approaches have the following accuracy.

1. Var(X)
2. 0:84Var(X)
3. 0:66Var(X)

We see that the third approach yields the best (smaller) MSE. However, note that this approach requires some global knowledge of the network topology, while the second approach requires only local knowledge.

B. An Efficient Continuous Neighbor Discovery Algorithm

Suppose that node u is in initial neighbor discovery state, where it wakes up every TI seconds for a period

of time equal to H, and broadcasts HELLO messages. Suppose that the nodes of segment S should discover u within a time period T with probability P. Finally, suppose that each node v in the segment S is in continuous neighbor discovery state, where it wakes up every $T_N(v)$ seconds for a period of time equal to H, and broadcasts HELLO messages.

We assume that in order to discover each other, nodes u and v should have an active period that overlaps by at least a portion $\partial, 0<\partial<1$ of their size H. Thus, if node u wakes up at time t for a period of H, node v should wake up between t-H(1- ∂) and t+H(1- ∂). The length of this validtime interval is 2H(1-∂). Since the average time interval between two wake-up periods of v is $T_N(v)$, the robability that u and v discover each other during a specific HELLO interval of u is

$\frac{2H(1-\partial)}{TN(v)}$

Let n be the number of in-segment neighbors of u. When u wakes up and sends HELLO messages, the probability that at least one of its n neighbors is awake during a sufficiently long time interval is

$1-(1-\frac{2H(1-\partial)}{TN(v)})^{n}$ consider a division of the time axis of u into time slots of length H. The probability that u is awake in a given time slot is $\frac{H}{TI}$ and the probability that u is discovered during this time slot is $P_1 = \frac{H}{TI}(1-(1-\frac{2H(1-\partial)}{TN(v)})^{n}$ Denote by D the value of $\frac{T}{H}$ Then, the probability that u is discovered within at most D slots is $P2= 1-(1-P1)^{D}$. Therefore, we seek the value of $T_N(v)$ that satisfies the following equation:

$$1 - (1 - P_1)^{D} \geq P$$

which can also be stated as

$$P_1 \geq 1 - \sqrt[D]{1-P}$$

Since $P_1 = \frac{H}{TI}(1-(1-\frac{2H(1-\partial)}{TN(v)})^{n}$, we get

$$\frac{H}{TI}(1-(1-\frac{2H(1-\partial)}{TN(v)})^{n} \geq 1 - \sqrt[D]{1-P}$$

and therefore

$$T_N(v) \leq \frac{2H(1-\partial)}{1-\sqrt[n]{1-\frac{T}{H}(1-\sqrt[D]{1-P})}}$$

Since v does not know the exact value of n, it can be estimated.

IV. CONCLUSION

We presented an algorithm for determining the wake-up frequency of the nodes in a sensor network. This

algorithm minimizes the energy consumption of the nodes and bounds the maximum delay on the routes from the nodes to the gateway. We simulated the algorithm over random sensor networks with different topologies and studied its impact on network energy consumption. This study revealed that the algorithm reduces the total energy consumption by 60- 70% compared to energy consumption under equal assignment.

V. REFERENCES

[1] R. madan and S. Lall,"An energy optimal algorithm for neighbor discovery in wireless sensor network,"Mob. Netw Appl.,vol.11,no.3,pp.317-326.2006.

[2] S. Vasudevan, J. Kurose, and D. Towsley, "On neighbour discovery in wireless networks with directional antennas," in INFOCOM, vol. 4, 2005, pp. 2502–2512.

[3] M. J. McGlynn and S. A. Borbash, "Birthday protocols for low en-ergy deployment and exible neighbour discovery in ad hoc wireless networks," in MobiHoc: Proceedings of the 2nd ACM International Symposium on Mobile Ad Hoc Networking and Computing. New York, NY, USA: ACM Press, 2001, pp. 137–145.

[4] R. Madan, Department of Electrical Engineering, Stanford University, Stanford CA 94305- 9505, U.S.A. ,An Energy-Optimal Algorithm for Neighbor Discovery in Wireless Sensor Networks.

[5] Wei Ye, John S. Heidemann, and Deborah Estrin. Medium access control with coordinated adaptive sleeping for wireless sensor networks. IEEE/ACM Trans. Netw., 12(3):493–506, 2004 .

[6] Gang Lu, Narayanan Sadagopan, Bhaskar Krishnamachari, and Ashish Goel. Delay efficient sleep scheduling in wireless sensor networks. In INFOCOM, pages 2470–2481, 2005.

[7] Gang Lu, Bhaskar Krishnamachari, and Cauligi S. Raghavendra. An adaptive energyefficient and low-latency mac for data gathering in wireless sensor networks. In IPDPS, 2004.

[8] Wei Lai and I. C. Paschalidis. Routing through noise and sleeping nodes in sensor networks: latency vs. energy trade-offs. In Proceedings of the 45th IEEE Conference on Decision and Control, pages 2716–2721, December 2006

[9] Abbas El Gamal and James Mammen. Optimal hopping in ad hoc wireless networks. In INFOCOM, pages 1–10, 2006.

Cross-layer Features Based Intrusion Detection System For Wireless Ad HOC Network

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ABSTRACT

A Mobile Ad hoc Network (MANET) is a network of mobile nodes which dynamically grouped to gather and establish arbitrary and temporary network topology. Ad hoc network is vulnerable to many kind of attack because of infrastructure less architecture. Cross layer based intrusion detection system (IDS) for wireless ad hoc networks using association rule mining and classification is our main focus in this paper. Specifically, features of MAC layer and network layer to profile normal behaviours of mobile nodes are used. The proposed CIDS is able to effectively detect an attack and is able to localize the attack source. False positive rate is reduced through the module 2 of the CIDS where intelligence gathered from neighbour nodes is used to make a collaborative decision by the monitor node. Our proposed solution will lead new track and work in the field of CIDS and eliminating other network attack like jelly fish.

Keywords – Association rule mining, CIDS, classification, jelly fish attack, MANET.

1. INTRODUCTION

An ad hoc network is a group of nodes connected gather by wireless links. Associations between nodes are established when they are in the vicinity of each other. All mobile nodes agree to relay each other's packets, and function as routers. While self-organizing nature of ad hoc networks provides convenient method for communication among mobile nodes. Main problem in ad hoc network is the lack of central authority which will restrict any node from doing misbehaviour by defining the privilege to individuals or which can monitor the traffic so it is very hard to detect the attack.

Attack on Ad hoc network may affect the wired network also. It is Because of hijacking of the legitimate node (station) by the malicious node by forming the ad-hoc network with that legitimate node.

Attack in ad hoc network can be applied on each individual layer of the network protocol stack. Because of lack of infrastructure the IDS used in wired network can not be used in wireless ad hoc network. Also the resource constrained environment may create problem for development of IDS. In this paper, we propose to use a rule-based data mining and classification techniques for anomaly detection to detect attacks on ad hoc networks with reduced feature set. Anomaly detection techniques are usually prone to high false positive alarm rates.

Our approach is to specify a reduced feature set across the MAC layer and the network layer to profile normal user behaviours. The proposed method aims at easing the complexity of the proposed IDS, and extending its detection ability to both layers.

2. RELATED WORK

In paper [1] author has used classification based technique for routing anomaly detection in the Ad hoc network. Their work was followed by the classification based approach on certain features at both MAC and Network layer. Authors have proposed new approach for the classification based on average probability(AP).Association rule based IDS[2] has been proposed for detecting the misbehaviour of the node. Authors have used Bayesian network to improve performance of the system. In paper [3], monitor based packet drop detection using cross layer detection is given. In this technique mobile node (who is in the vicinity of the attacker) with sufficient energy will work as a monitor and detect the attacker by sending packet and detecting the reply from that malicious node. Author of paper [4] has given a Support vector machine (SVM) based method for sinking behaviour identification using cross layer features.

Our focus will be on anomaly detection with data mining based approach. Few methods based on data mining of database have been already proposed by researchers in [1][2]. Association rule mining is the process of capturing rules from given data based on support threshold and confidence threshold for selected rules with respect to minimum support and minimum confidence.

- **Classification of IDS**

Most of the IDS suggested previously by the researcher in [1]-[7] can be classified into below four category.

1) Agent based intrusion detection system.
2) Group based intrusion detection system.
3) Cluster based intrusion detection system.
4) Cross layer Intrusion detection system.

Because of changing topology and movement of the node some time it is very hard to relies on a single-layer detection method because there is not enough evidence using single layer detection. As a result, the concept of multi-layer or cross-layer detection mechanism is raised and discussed in [3] and [4]. IDS proposed previously have architecture consist of four modules: data gathering, profile generation, Anomaly detection and decision tacking system.

Data Gathering: this module collects audit data (network activities) from a given network in normal condition within its observable radio transmission range.

Profile Generation: this module has two subsystems:

1) **Data preparation:** here the collected data are prepared for creating normal behaviour profile. Processes like filtering, aggregation, data suppression are applied here.
2) **Profiler (Profile generator)**: the second phase is made up of several techniques like clustering, classification rule mining or SVM where normal profile is made by the pre processed data. A normal profile is an aggregated rule set of multiple training data segments.

Anomaly Detection: This phase detect anomaly in the network with the help of derived rule set in this module, test data profiles are compared with the expected normal profiles. Any rules with deviations beyond a threshold interval are considered as anomalies. Suppose some rule generated from test data was not previously available in normal profile then it will be detected as anomaly, it is considered as an anomaly rule; if the rule is in the rule set, but its support and confidence level is beyond the interval [minimum − threshold, maximum+ threshold], the pattern described by the rule becomes unusual, and is consider as an anomaly rule [2].

Decision Tacking System: when any anomaly rule trigger that will be attended locally as well as globally by giving alert to the neighbours when the support and confidence of anomaly rule goes above tolerated level. Here are some attack those are possible at different layer.

Layer	Type of Attack
Physical	Jamming, Tampering
Data link	Collision, Exhaustion, Unfairness, Jamming
Network & routing	Neglect and Greed, Homing, Misdirection, black hole, packet drop.
Transport	lFlooding, Desynchronization

Table 1. Classification of attack at different layer. [5]

3. PROJECT BODY

3.1. Problem Statement:

In the mobile ad hoc network nodes can directly communicate with all the other nodes within their radio ranges; whereas nodes that not in the direct communication range use intermediate node(s) to communicate with each other. Here are some basic features of MANET which cause threat to the security of the MANET.

Unreliability of wireless links between nodes: Because of the limited energy supply for the wireless nodes and the mobility of the nodes, the wireless links between mobile nodes in the ad hoc network are not consistent for the communication participants. And any malicious node can communicate with the node which is in the in the vicinity of that node.

Non uniform topology: Due to change in the position of mobile nodes, the routing information will be changing all the time.

Lack of power supply: because of energy constrained environment in ad hoc network the node will be rely on battery power. Any malicious node can easily attack the node by attacking the power of the node by making node busy in bogus communication and some time leads the victim node to the off state. This cause DOS (denial of service) type of attack.

Because of above listed futures ad hoc network is vulnerable to some serious type of attacks there for we need to pay more attention to the security issues in the mobile ad hoc networks.

So our main objectives are:

- How to prevent and detect malicious activity of the node in the ad hoc network?
- How to increase the throughput of the system?
- How to reduce overall delay in routing mechanism?

3.2 Evaluation Metrics

The evaluation metrics consist of following things.

Throughput	The overall output of the system that goes down because of malicious activity of node
Delay in routing	Total delay produced in packet or data delivery because of malicious node.
Overhead	Extra work that nodes have to compute for routing because of malicious activity of the node.

3.3. Feature of interest

There are many type of features available at both MAC as well as network layer. According o the need of efficiency and effectiveness different feature set can be taken.

At network layer IP packets can be categorised in to two type 1) control packets (i.e. Route Request, Route Reply, Route Error) and 2) data packets. We combine all routing control packets into one category as routing Control packet (CtrlPkt) , and name IP data packet as routing data packet (DataPkt). Thus the payload in a MAC data frame contains either a CtrlPkt or DataPkt. In summary, we present our proposed feature set and its value space as below. We are also interested in packet delivery ratio and delay to the packet because of queue buffering.

Table 2. The proposed feature set

Feature	Value Space
Direction of the packet	: SEND, RECV, DROP
Source address (SA)	: sai, $\forall i \in$ node set S
Destination address (DA)	: daj , $\forall j \in$ node set S
Type of data	: RTS, CTS, DATA, ACK,
Packet type	: DataPkt , CtrlPkt
Delay	: in form of second
Package drop	: percentage of packet drop
Route related features	: route add - remove, total route change, avg route length

3.4. Proposed Architecture.

Our work follows existing data mining techniques like association rule mining and classification for detecting anomaly. Some intrusion detection techniques suggested in literature use probabilistic analysis where the resulting models are not straightforward to be re-evaluated by human experts [2]. Some data mining models require temporal sequence from data stream, which is domain specific and highly inefficient when a large feature set is involved [2]. Because of large feature set data availability of MANET we can use different combination of feature to correlate them.

In given paper, a cross feature based anomaly detection algorithm is given in phase 2. Formally speaking, in the cross-feature analysis approach, aim is to establish correlations between eachfeature and all other features. i.e., try to solve the classification problem $\{f1, f2, \ldots, fi-1, fi+1, \ldots, fL\} \rightarrow fi$ where $\{f1, f2, \ldots, fL\}$ is the feature vector [1]. Note that in the machine learning area, the terminology class in a classification system represents the task to be learned based on a set of features, and the class labels are all possible values a class can take [1]. Thus, the anomaly detection problem can be transformed into a set of classification sub-problems, where each sub- problem chooses a different feature as a new class label and all other features from the original problem are used as the new set of features. The outputs of each classifier are then combined to provide an anomaly detector. The new model of CIDS can be used as an effectively to reduce anomaly.

Our main object is to identify the normal and abnormal profile with selected feature set and detect the anomaly in the network. It consists of two phases CIDS Phase -1, CIDS Phase-2.

CIDS Phase -1

CIDS phase -1 works for collection of data and use it as a training data set to generate normal behaviour.

By applying the association rule mining we will mine the packet level event, which contains <Timestamp, Dir, SA, DA, PktType>. An example association rule is (sa5, DataPkt → da12, RECV), (0.4, 1), which describes an event pattern related to the RECV flows of the monitoring node. Here the support of rule is 0.4(40%). That is , 20% of transaction records matches the event of "node 5 sends data packets to node 12", and confidence 100% suggest that when node 16 receives data packets, they are 100% of the time from node 7. and then prune the rules with MFI criteria. MFI is defined as a frequent item set for which none of its immediate supersets are frequent [2]. This pruning process dramatically reduces the size of normal profile, yet still captures the frequent association patterns from a data set. In our experiments, the MFI pruning can reduce the number of association rules by 20 to 40%. Once association rules are extracted from multiple segments of a training data set, they are then aggregated into a rule set, which is considered as a normal profile. After extracting the Rule set the process continuously train the rules to certain amount of time. This process gives the average rule set values (support and confidence) at the normal behaviour (normal profile) of network without attack. when the attach is there in the network all the nodes which has higher threshold value for packet sending rate then avg(threshold) will be kept in non-trusted region.

We also train a classification model for CIDS phase-1, Here we are defining classes Ci : {f1, . . . , fi−1, fi+1, . . . , fL} → {fi}. For normal events, the prediction by Ci is very likely to be the same as the true value of the feature; however, for anomalies, this prediction is likely to be different. Because Ci is trained from normal data, and their feature distribution and pattern are assumed to be different from those of anomalies. This implies that when normal vectors are tested against Ci, it has a higher probability for the true and predicted values of fi to match. Such probability is significantly lower for abnormal vectors. With the help of degree matching we can distinguish between normal and abnormal behaviour. We name the model defined above a sub-model with respect to fi [1]. Obviously, relying on one sub-model with respect to one labelled feature is insufficient. Therefore the model building process is repeated for every feature and up to L sub- models are trained [1].

Data: feature vectors of training data **f1**, . . . , **fL**.
Result: classifiers **C1**, . . . , **CL**.

begin

$\forall$ i, train Ci : { f1, . . . , fi−1, fi+1, . . . , fL} → fi;

return C1, . . . , CL;

end

Where Ci(x) is the predicted value from sub-model with respect to fi.

Algorithm 1: Cross-Feature Analysis: Training Procedure [1].

By analysing the flow of network we can predict that the network is under some malicious activity or not with the help of normal traffic rate observed in association rules. When there is abnormal traffic at some point those nodes will be considered as possibly malicious and kept in non-trusted region. Now the monitor node will execute the CIDS module-2, and try to detect whether the node in non trusted region is exactly malicious or not. For that the classification technique of data mining is used. Monitor node is selected on the cluster based technique. Group of nodes which are within certain vicinity of victim node will form a cluster among themselves. Where one node will work as cluster head and that node will execute CIDS module 2. Selection of the cluster head will be based on the energy level of the cluster node. Some node might be selfish and will refuse to work as monitor. Here we assume that each node with sufficient energy will be having equal chance to work as cluster head and elected randomly.

CIDS phase-2

An event is classified as anomaly if and only if the average probability is below the threshold. Assume that p(fi(x)|x) is the estimated probability for the true class of the labelled feature average probability is the average output value of probabilities associated with true classes over all classifiers. The optimized version is shown in Algorithm given below.

Data: classifiers C1, . . . , CL, event x = (f1, . . . , fL), decision threshold θ;

Result: either normal or anomaly;

begin

AvgProbability ← i p(fi(x)|x)/L;

if AvgProbability ≥ θ then return “normal”;

else return “anomaly”;

end

Algorithm 2. Verification of malicious node. [1]

3.5. Methodology.

We are trying to show the effect of malicious activity on through put of network. We have implemented the jelly fish attack with ns-2 and try to check the trough put which goes down due to malicious activity of the nodes. The jelly fish attack can be implemented by creating malicious node and increasing the delay of packet forwarding or by dropping the packet from the malicious node.

Table 3. Parameters for the simulation are as follows.

Area	2000m X 2000m
Nodes	50
Packet size	512
Transmission protocol	UDR

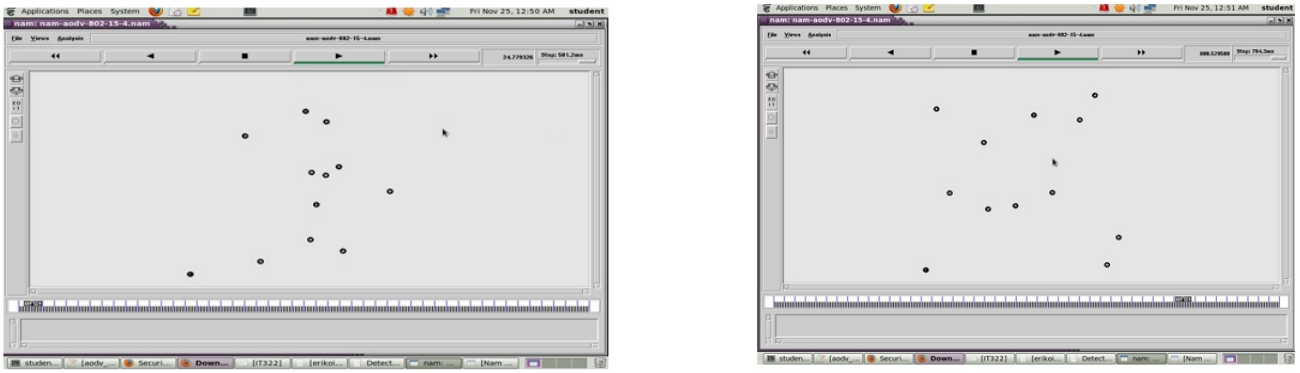
Application traffic	CBR
Transmission rate	10 Mbps
Pause time	24.73
Maximum speed	31 sec
Propagate model	Radio propagation
Maximum malicious node	50
Type of attack	Delayed forwarding
Examination	AODV

3.6. Expected results of IDS:

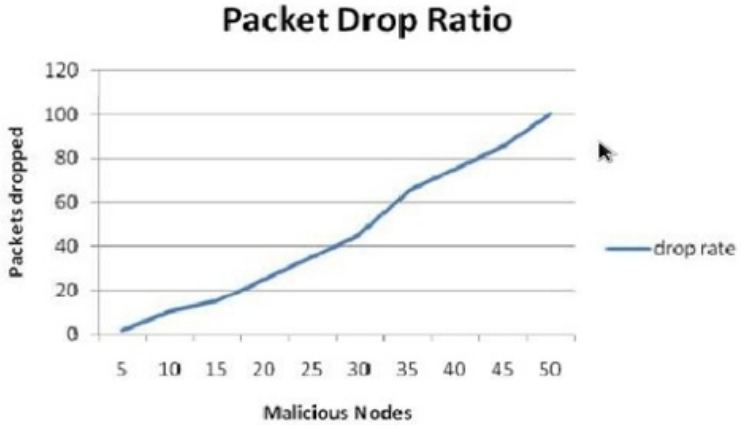
Proposed algorithm is the mixture of two analysis techniques association rule mining and classification. All threat will be detected in the first phase of the CIDS phase-1 where network flow is tested. With the help of CIDS phase -2, we are verifying the malicious activity of the targeted node. So the overall effect of malicious node is taken in to consideration by analysing traffic at network and MAC layer which will result into greater probably of Intrusion Detection.

4. RESULTS AND ANALYSIS:

Screen shot of 12 nodes randomly moving the screen in random direction and getting communicated with each other when the come at the vicinity of each other.



Screen shot of 12 nodes randomly moving at time 800ms.



It is seen from the graph that when malicious node is introduced in the network the overall throughput will goes down by the malicious activity of node because packet drop ration increase with increase of malicious activity.

5. CONCLUSION

In this paper we have presented a cross-feature based anomaly IDS for ad hoc networks using unsupervised association rule mining and classification technique. Here we have tried to reduce the false alarm rate by using classification technique, and also try to reduce the number of redundant alerts.

6. REFERENCES:

1. *Y. Huang, W. Fan, W. Lee, "Cross-Feature Analysis for Detecting Ad-Hoc Routing Anomalies," In proc of. 23rd International Conference on Distributed Computing Systems, 2003.*
2. *Y. liu, Y. Li,H. Man, " Short Paper: A Distributed Cross-Layer Intrusion Detection System for Ad Hoc Networks", In proc of. The First International Conference on Security and Privacy for Emerging Areas in Communications Networks,2005.*
3. *G. Li,J. He, Y. Fu, " A Group-based Intrusion Detection Scheme in Wireless Sensor Networks" The 3rd International Conference on Grid and Pervasive Computing – Workshops, IEEE, page no -286-291,2008.*
4. *J. John, B. Lee,A. Das, "Cross-Layer Detection of Sinking Behavior in Wireless Ad Hoc Networks Using SVM and FD", IEEE TRANSACTIONS ON DEPENDABLE AND SECURE COMPUTING, VOL. 8, NO. 2,pg. no 231-245, MARCH-APRIL 2011.*
5. *S.Bose and A.Kannan ,"Detecting Denial of Service Attacks using Cross Layer based Intrusion Detection System in Wireless Ad Hoc Networks", IEEE-International Conference on Signal processing, Communications and Networking,page no.82-188, 2008.*
6. *G. Helmer, J. Wong, V. Honavar, L. Miller and Y. Wang, "Lightweight Agents for Intrusion Detection." Journal of Systems and Software, Elsevier. Vol. 67. No. 1. pp. 109- 122, 2003.*
7. *G. Thamilarasu, A. Balasubramanian2, S. Mishra2 and R. Sridhar, "A Cross-layer based Intrusion Detection Approach for Wireless Ad hoc Networks", MASS 2005 Workshop - WSNS05,IEEE,2005.*
8. *H. Yang, H Luo, F. Ye; S. Lu, L. Zhang, "Security in mobile ad hoc networks: challenges and solutions," IEEE Wireless Communications, Volume: 11 Issue: 1, page no. 38-47, Feb 2004.*

FPGA Implementation of UART Controller with Automatic Baud Rate Generator

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ABSTRACT

Universal Asynchronous Receiver and Transmitter (UART) allows full-duplex communication in serial link and has been widely used in the data communications. It provides a way of serial communication, between two devices but whilst there is a need to provide communication between two devices that are operating at different baud rates, it is intricate to provide communication with an UART. It is a kind of serial communication protocol, mostly used for short-distance, low speed, low-cost data exchange between computer and peripherals. Specific interface chip will cause waste of resources and increased cost. In this, we present a design method of asynchronous FIFO and structure of the controller with automatic baud rate detection. This controller is designed with FIFO circuit block and UART circuit block within FPGA to implement communication in modern complex systems quickly and effectively. Here we use VHDL to implement the UART core functions and integrate them into a Sparten 3E FPGA chip to achieve compact, stable and reliable data transmission. In the result and simulation part, we will focus on baud rate generation at different frequencies and check the receive data with error free. The Baud Rate Generator is incorporated into the UART design. This frequency divider will automatically adjust according to requirements.

Keywords – UART, Baud rate generator, Shift Register, FIFO

1. INTRODUCTION

Asynchronous serial communication has advantages of high reliability, less transmission line and long transmission distance, therefore is widely used to exchange data between a computer and external devices.

Asynchronous serial communication is implemented by UART. It provides full-duplex communication in serial link; this has been widely used in the data communications. UART includes a transmitter and a receiver. Transmitter controls transmission by taking a data word in parallel format and directing the UART to transmit it in a serially. Likewise, the Receiver must detect transmission, receive the data in serially, and store the data word in a parallel format. The conversion of serial to parallel data is handled by UART. Serial communication reduces the distortion of a signal; therefore data transfer is possible between two systems separated by great distance. The UART serial module is divided into three sub-

modules: the baud rate generator, receiver module and transmitter module. The baud rate generator is used to produce a local clock signal. In data transmission through the UART, once the baud-rate has been established, both the transmitter and the receiver‟s internal clock are set to the same frequency. TXD is the transmit side, i.e. the output of the UART; RXD is the receiver, i.e. the input of the UART. The UART receiver module is used to receive the serial signals at RXD and convert them into parallel data. The UART transmit module converts the data bytes into serial bits according to the frame format and transmits those bits through TXD.

2. LITERATURE REVIEW

FANG Yi-Yuan CHEN XUE- Jun has presented a paper on “Design and simulation Of UART serial communication Module Based on VHDL”. In this paper they presented that the UART is the microchip with programming that controls a computer's interface to its peripherals. It is the most widely used serial data communication circuit ever. The whole process of serial transmission is based upon the principle of the shift register. There are two primary forms of serial transmission that are Synchronous & Asynchronous. In Synchronous serial communication requires that the sender and receiver should work on the same clock with one another. Asynchronous transmission allows data to be transmitted without sending a clock signal to the receiver. This design uses VHDL as the design language to achieve the modules of the UART.

The results are reliable & stable. The design has high integration, great flexibility with some reference value [1].

Shouqian Yu, Lili Yi, Weihai Chen, Zhao Jin Wen presented a paper on “Implementation of a Multi-channel UART Controller Based on FIFO Technique and FPGA”. In this paper they have presented that in several systems such as high data collection system, a high speed control system based on PCI and multi-DSP signal processing system, FIFO is used for complete communication between high speed device and low speed device or to complete communication between the same sub controllers. FIFO is the most important part of these systems and it works as a bridge between different devices. At the same, in our controller, asynchronous FIFO based on FPGA is also the most important part. So the features and capabilities of the asynchronous FIFO determine the features of our controller. The FIFO can be used to complete communication in parallel or serial port [2].

Bhavana Mahure and Rahul Tanwar have presented a paper on “UART with automatic baud rate generator and frequency divider”. In this paper they have presented that the most commonly used numbers of data bits of a serial connection are eight, which corresponds to a byte. When a regular ASCII

code is used in communication, only seven LSBs are used and the MSB is 0. If the UART is configured as 8 data bits, 1 stop bit, and no parity bit, the received word is in the form of 0-dddd-ddd-0-1, in which d is a data bit and can be 0 or 1. Assume that the UART configuration is 8 data bits, 1 stop bit, and no parity bit, and the baud rate can be 4800, 9600, or 19,200 baud [3].

The circuit produces Frequency Division as it now divides the input frequency by a factor of two. Frequency Divider is dividing the frequency according to system requirement. So we can use this UART with frequency divider, no need to attach another device in that system to divide the frequency.

Nurul Fatihah Jusoh, Azlina Ibrahim, Muhamad Adib Haron and Fuziah Sulaiman presented a paper on "An FPGA Implementation of Shift Converter Block Technique on FIFO for UART" the paper represents the implementation of the bidirectional shift converter technique with FIFO circuit block and UART circuit block through FPGA device using Verilog HDL language to be applied in embedded system converter RS232 to USB (Universal serial bus) [4].

Nennie Farina Mahat presented a paper on " Design of a 9-bit UART Module Based on Verilog HDL." In this paper, a modified UART design is proposed with automatic address indicated, which is called 9-bit UART [5]

"Platform-Independent Customizable UART Soft-Core" Biplab Roy. In this paper, we propose a technique for software implementation of a UART using shift register with the goal of getting a customizable UART-core which can be used as a module in implementing a bigger system irrespective of one's choice of the implementation platform [6].

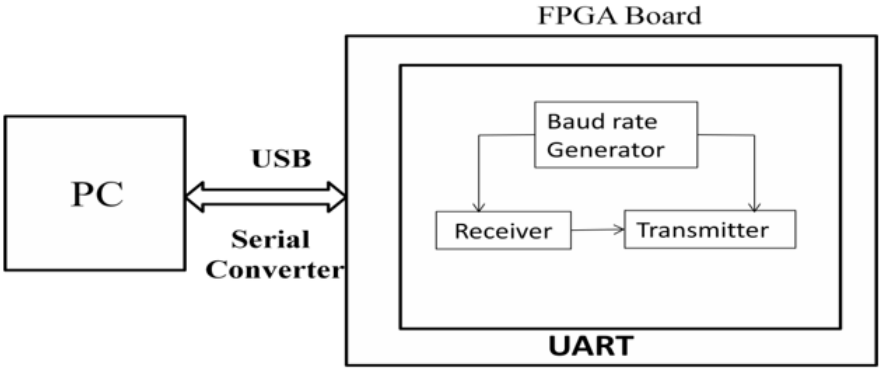

Fig.1. Block diagram of interfacing of PC with FPGA Board.

3. METHODOLOGY

There are two primary forms of serial transmission: Synchronous and Asynchronous. They are:

1. UART Universal Asynchronous Receiver/Transmitter

2.USART Universal Synchronous-Asynchronous Receiver

Asynchronous serial communication is usually implemented by UART. The Universal Asynchronous Receiver/Transmitter (UART) controller is the key component of the serial communications of a computer.

In Serial communication, there occurs, reduction of the distortion of a signal; therefore it is possible to make data transfer between two systems at great distance It enables to control the conversion between serial and parallel data. The UART serial communication module is divided into three sub-modules: the baud rate generator, receiver module and transmitter module.

The transmitter is a distinctive shift register that loads data in parallel, then at a specific rate it shifts out bit by bit. On the other hand The receiver shifts the data bit by bit and then rearrange the data. UART transmitter controls communication by getting a data word in parallel format & directing the Universal Asynchronous Receiver Transmitter to transmit it in a serial format.

Receiver Module

During the UART reception, the serial data and the receiving clock are asynchronous, so it is very important to correctly determine the start bit of a frame data. The receiver module receives data from RXD pin. RXD jumps into logic 0 from logic 1 can be regarded as the beginning of a data frame. The start bit is identified by detecting RXD level changes from high to low. The serial receiver module includes receiving, serial and parallel transform, and receive caching, etc . The function of the receiver module is that it will store the tx_out i.e. the output of the transmitter which is of single bit into the intermediate register with the start bit as the least significant bit and collectively provides the serial data of 8. When the load signal is high it will get the start bit from the transmitter which assures that the original data is now being send by the transmitter. Once the shift signal is becomes high with no load signal, the data coming from the transmitter gets shifted into the intermediate register of the receiver and provides the 8 bit serial data which we have given as an input to the transmitter.

Trasmit Module

The function of transmit module is to convert the sending 8-bit parallel data into serial data, adds start bit at the head of the data as well as the parity and stop bits at the end of the data. When the UART transmit module is reset by the reset signal, the transmit module immediately enters the ready state to send. The function of the transmitter module is to convert the 8 bit serial data into the single bit data. In this module, when our load signal is high the data_in is stored into the holding register. The data in the holding register is shifted to the intermediate register with the start bit of zero and this intermediate register is of 9 bits. Once the shift signal is high the least significant bit of the intermediate register i.e. the start bit comes at the output of the transmitter and served as the input to the receiver. When the entire data has been sent, the transmitter provides a parity bit which is served as the input to the receiver.

5. IMPLEMENTATION AND RESULTS

The design of automatic baud rate generator is coded using VHDL language. Simulation and synthesis of UART is done on ModelSim software and Xilinx ISE software respectively. We implemented the UART controller with automatic baud rate generator on a Xilinx XC3S500E Spartan-3E FPGA kit.

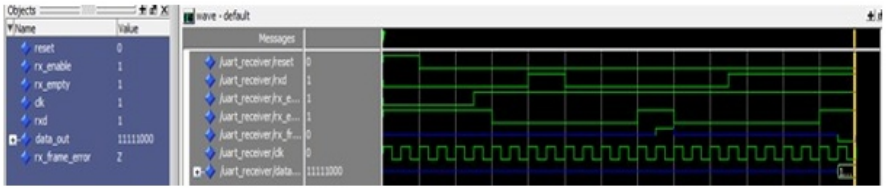

Fig2 : Output of Receiver

If the system has a signal reset active then reception is high impedance while other status signal i.e rx_enable is „1" and rx_empty will be „1". When system has reset =0 and reception signal is enable (rx) then data reception is started. For every rising edge of clock pulse individual data bit is received by the receiver module as UART protocol states first bit is 0, then remaining 8 bit are data bit last bit is 1 then successful reception of data has been occurred. If start bit is not „0" then all remaining data has been discarded by receiver module by indicating rx_frame error="1".

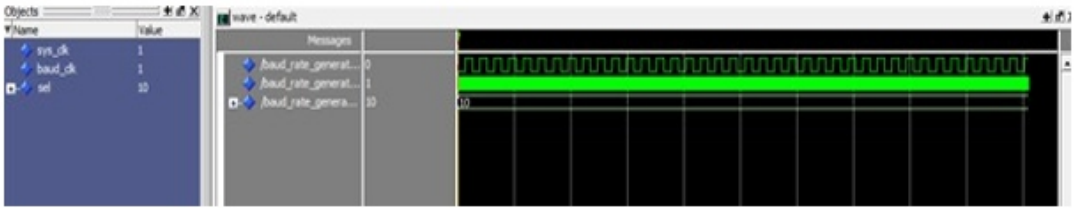

Fig3: Output of Baud Rate Generator

Fig shows the simulated waveform for the baud rate 19200. First we set the system clock at „1". We have four combinations for select lines that are 00,01,10,11. From these four options we can obtain four different baud rates and default baud rate generated is 9600. In above waveform we have set the system clock at "10", so 19200 baud rate is generated.

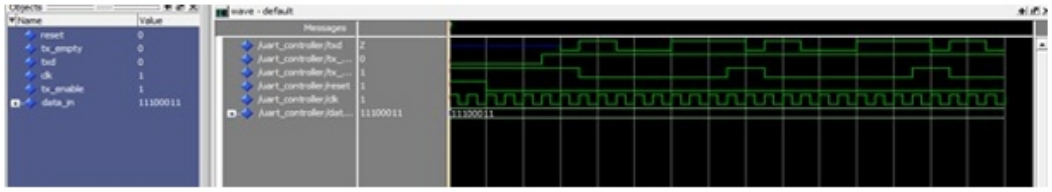

Fig4: Output of Transmitter

If the system has a signal reset active then reception is high impedance then data transmission has been occurred, while other status signal i.e rx_enable is „0" and rx_empty is „1".

When system reset is „0", rx enable is „1" and rx empty is „0"then data bit has been given out at every rising edge of the clock at txd line. First starting bit has been send as „0" on txd line then parallel data has been send at every rising edge of cock. After completion of successive & data bits , stop bit has been send as" 1".

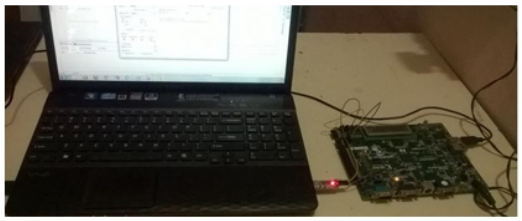

Fig Peripheral connected to FPGA Board

Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	89	9,312	1%	
Number of 4 input LUTs	195	9,312	2%	
Number of occupied Slices	134	4,656	2%	
Number of Slices containing only related logic	134	134	100%	
Number of Slices containing unrelated logic	0	134	0%	
Total Number of 4 input LUTs	259	9,312	2%	
Number used as logic	194			
Number used as a route-thru	64			
Number used as Shift registers	1			
Number of bonded IOBs	13	232	5%	

Fig. 4 Synthesis result of UART controller.

Our results for FPGA Altera‟s Cyclone II FPGA:

EP2C5F256C6 our ref clock : 50MHz

	Baud Rate Generator	Transmitter	Receiver
Logic Elements	48	24	39
Registers	33	14	31
I/O pins	2	12	13

CONCLUSION

Efficient implementation of UART with automatic baud rate generator of Sparten 3E board is presented in this paper. High throughput is achieved in this design In this we had added the concept of automatic baud rate detection, so when the transmitter changes the baud rate the receiver can adjust automatically and it reduces the delay for the reception of data than the fixed baud rate. Especially in the field of electronic design technology has recently become widely used, this design shows great significance.

REFERENCES

1. *FANG Yi-Yuan CHEN XUE- jun , "Design and simulation Of UART serial communication Module Based on VHDL",2011.*
2. *Shouqian Yu ,Lili Yi, Weihai Chen, Zhao jin Wen," Implementation of a Multi-channel UART Controller Based on FIFO Technique and FPGA", 2007*
3. *Bhavna Mahure and Rahul Tanwar (2012) "UART with Automatic Baud Rate Generator and Frequency Divider". Journal of Infor-mation Systems and Communication, ISSN: 0976-8742 & E- ISSN: 0976-8750, Volume 3, Issue 1, pp.- 265-268.*
4. *Fatihah Jusoh, Azlina Ibrahim, Muhamad Adib Haron and Fuziah Sulaiman "FPGA Implementation of Shift Converter Block Technique on FIFO for UART",2011 Nennie Farina Mahat, " Design of a 9-bit UART Module Based on Verilog HDL.",2012*
5. *Bipla Roy,"Platform-Independent Customizable UART Soft-Core",2012*
6. *Jan Henning Mueller, Mojdeh Hamzavi Nejad Moghaddam, Bastian Mohr, Sebastian Strache,Ralf Wunderlich and Stefan Heinen, "An Adaptable UART Based Configuration and Read-out Interface for IC Prototypes",2012*
7. *Mohd Yamani Idna, Idris Mashkuri Yaacob, "A VHDL Implementation of BIST Technique in UART Design",2003*
8. *J. Norhuzaimin and H.H Maimun, "The Design of High Speed UART",2005*
9. *Shihua Tong, "Design and Simulation Analysis of UART IP Core",2011*
10. *Naresh Patel, Vatsalkumar Patel, Vikaskumar Patel, "VHDL Implementation of UART with Status Register"*
11. *Dr. Garima Bandhawarkar Wakhle," Synthesis and Implementation of UART using VHDL Codes",2012*
12. *Ritesh Kumar Agrawal, Vivek Ranjan Mishra," The Design of High Speed UART",2013*

Dual Tone Multiple Frequencies Controlled by Painting Robot

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ABSTRACT

Conventionally, wireless-controlled robots use RF circuits, which have the drawbacks of limited working range, limited frequency range and limited control. Use of a mobile phone for robotics control can overcome these limitations. In this Project DTMF Controlled by Painting Robot technique is used. "DTMF is capable of receiving a set of command (instructions) in the form of DTMF tones and performs the necessary actions of the robotic moments like forward, backward, left, right, stop, up and down functions are controlled by a mobile phone that makes a call to the mobile phone attached to the robot. In the course of a call, if any button is pressed, a tone corresponding to the button pressed is heard at the other end of the call. Here tone is DTMF. It stands for "Dual Tone Multiple Frequencies". ARM7 controller perceives this DTMF tone with the help of the phone. The received tone is processed by the microcontroller with the help of DTMF decoder. The decoder decodes the DTMF tone into its equivalent binary digit and this binary number is sent to the microcontroller. The microcontroller is pre-programmed to take a decision for any given input and outputs its decision to motor drivers in order to drive the motors for forward or backward motion or a turn or Robotic hand need to move up and down and sprinkle water. The mobile that makes a call to the mobile phone stacked in the robot acts as a remote. DTMF signaling is used for telephone signaling over the line in the voice-frequency band to the call switching centre. The version of DTMF used for telephone tone dialing is known as „Touch-Tone." DTMF assigns a specific frequency (consisting of two separate tones) to each key so that it can easily be identified by the electronic circuit. The signal generated by the DTMF encoder is a direct algebraic summation, in real time, of the amplitudes of two sine (cosine)waves of different frequencies, i.e., pressing „5" will send a tone made by adding 1336 Hz and 770 Hz to the other end of the line. Because recording DTMF tones and play back will be control painting/spraying automatically.

Keywords – DTMF (Dual Tone Multiple Frequency), RF, ARM7 controller, Touch-Tone

1. INTRODUCTION

Wall painting, conventionally, has been carried out by human hands on scaffolds provisionally built around a subject wall. This, however, not only is a kind of work performed on dangerous elevated spots and in unclean environment but also requires extra wok to take down the scaf- folds, thus often making it difficult to shorten a construction term or to reduce cost. There were some robots available on the markets which were, however, able to perform painting in a single color. Few of them had wide

applicability and their use was rather limited depending on a structure applied. Further, prior to drawing of a picture, a rough sketch needs to be prepared on a wall, taking much time for drawing the original picture as being enlarged. The actual targets for development of the wall painting robot, in order to solve the aforementioned situation, were set as follows are to improve safety by eliminating works on scaffolds, to make machine structure simple to enable easy mounting, to perform not only painting in a single color but also drawing in multiple colors and to be usable not only on external walls of structures but also in various other places such as on walls of civil structures.

1.1 Block Diagram Description

This block diagram consists of LPC2148 Microcontroller, DTMF Decoder, L293D (Driver IC), ULN2003, Relays, water pump motor. The power supply is connected to Microcontroller and DFMF Decoder output is connected to the Microcontroller. Microcontroller is connected to the L293D enable pins, the output of L293D is connected to the motors and ULN2003 via relay is connected to the water pump motor. The Microcontroller which is the heart of the project is used to control the devices like forward, backward, right, left spraying, stop etc., We can drive the ap- pliances with the help of IC drivers, which drives the relays etc. We are using drivers here to amplify low current signals to high current signals, as the output of Microcontroller is about 1 to 2 mA and this is not sufficient to drive some circuits which require input 10 mA of current. The following block diagram of LPC2148 ARM-7 Micro Controller as shown below Fig: 1.1

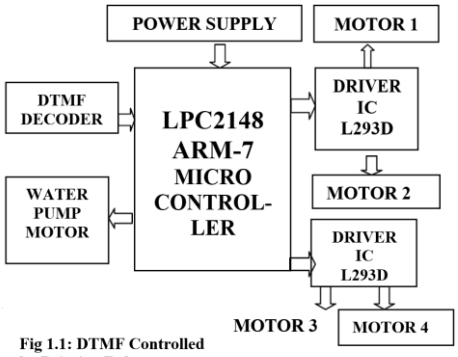


Fig 1.1: DTMF Controlled by Painting Robot

1.2 Schematic Diagram:

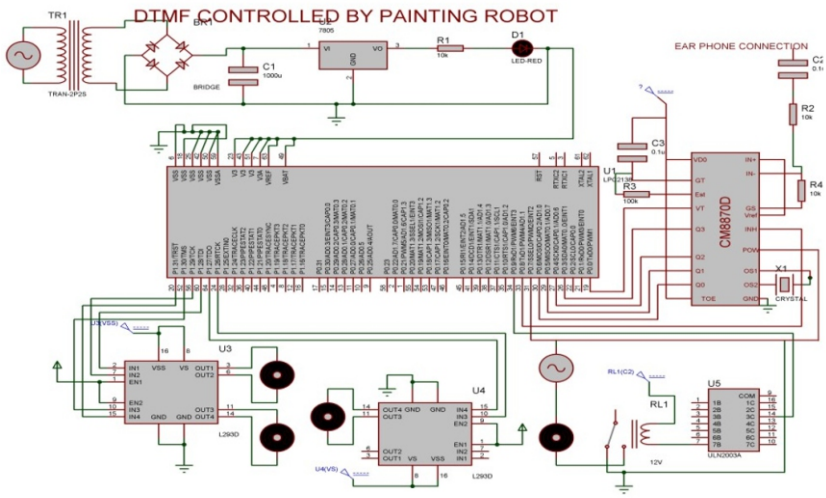


Fig 1.2: DTMF Controlled by Painting Robot Schematic Diagram

Here we used an embedded system architecture can be represented as a layered architecture as shown in Fig. 1.3. The operating system runs above the hardware, and the application software runs above the operating system. The same architecture is applicable to any computer including adesktop computer. However, there are significant differences. It is not compulsory to have an operating system in every embedded system.

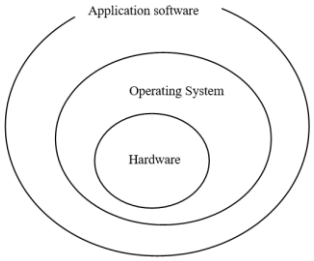


Fig 1.3: Layered Architecture of an Embedded System

1.3 ARM7 MICROCONTROLLER

The LPC2148 micro controllers are based on a 32/16 bit ARM7TDMI-S CPU with real-time emulation and embedded trace support, that combines the microcontroller with embedded high speed flash memory ranging from 32 kB to 512 kB. A 128-bit wide memory interface and unique accelerator architecture enable 32-bit code execution at the maximum clock rate. For critical code size applications, thealternative16-bit Thumb mode reduces code by more than 30 % with minimal performance penalty. Due to their tiny size and low power consumption. A blend of se- rial communications interfaces ranging from a USB 2.0 Full Speed device, multiple UARTs, SPI, SSP to I2Cs, and on-chip SRAM of 8 kB up to 40kB,make these devices very well suited for communication gateways and protocol converters, soft modems, voice recognition and low end imaging, providing both large buffer size and high processing power. Various 32-bit timers, single or dual 10-bit ADC(s), 10-bit DAC, PWM channels and 45 fast GPIO lines with up to nine edge or level sensitive external interrupt pins make these microcontrollers particularly suit- able for industrial control and medical systems. It is most widely 32-bit Architecture. The main difference between 8051 and ARM is 8051 is based on CISC design where as ARM is based on RISC design. In ARM all most all instructions will execute in single machine cycle.

1.4 LPC2148 Processor Features:

16- bit/32-bit ARM7TDMI-S microcontroller in a tiny LQFP64 package.8 kB to 40 kB of on- chip static RAM and 32 kB to 512 kB of on-chip flash memory. 128-bit wide interface/ accel-erat -or enables high-speed 60 MHz operation. In-System Programming/In-Application Pro- gramming (ISP/IAP) via on-chip boot loader software. Single flash sector/full chip erase in 400 ms and programming of 256 bytes in 1 ms. USB 2.0 Full-speed compliant device controller with 2 kB of endpoint RAM. In addition, the LPC2146/48 provides 8 kB of on-chip RAM ac- cessible to USB by DMA.One or two (LPC2141/42 vs. LPC2144/46/48) 10-bit ADCs provide a total of 6/14 analog inputs, with conversion times as low as 2.44

µs per channel.Single 10-bit DAC provides variable analog output (LPC2142/44/46/48 only). Two 32-bit timers/external event counters (with four capture and four compare channels each), PWM unit (six outputs) and watchdog. Low power Real-Time Clock (RTC) with independent power and 32 kHz clock in- put. Multiple serial interfaces including two UARTs (16C550), two Fast I2C-bus (400 kbit/s), SPI and SSP with buffering and variable data length capabilities. Vectored Interrupt Controller (VIC) with configurable priorities and vector addresses. Up to 45 of 5 V tolerant fast general purpose I/O pins in a tiny LQFP64 package. Up to 21 external interrupt pins available. 60MHz maximum CPU clock available from programmable on-chip PLL with settling time of 100µs.On-chip integrated oscillator operates with an external crystal from 1 MHz to 25 MHz. Power saving modes include Idle and Power-down. Individual enable/disable of peripheral functions as well as peripheral clock scaling for additional power optimization.

1.5 Board Features:

- Processor: LPC2148
- 2xSerial ports(One for ISP and other for Serial Communication)
- 12.00 MHZ crystal
- On board Reset Circuit with a switch.
- Dual Power supply (either through USB or using external power adapter).
- Power on LED supply.
- Three on-board voltage regulators 1.8V, 3.3V and 5V with up to 800mA current
- Extension headers for µC ports.
- Graphic LDC display interfacing port.
- USB Ports.
- CAN controller Interfacing.
- MMC/SD card interfacing.
- 8 Bit LED interfacing.
- EEPROM Interfacing.
- On board UART.

Connectors:

- Mini-B USB connector to UART#0 UART-to-serial bridge)

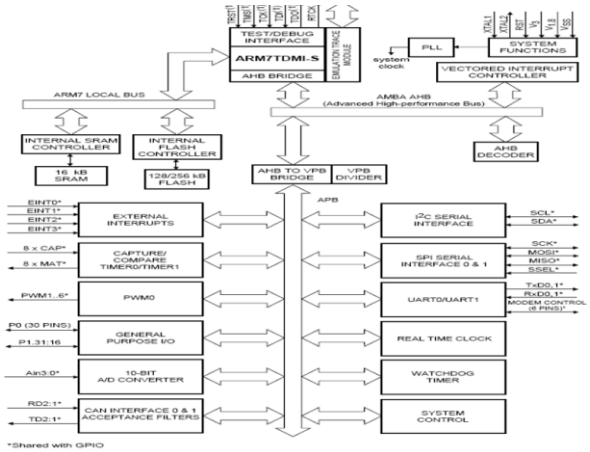


Fig 1.4: Arm-7 Block diagram

- Mini-B USB connector to LPC2148 device interface
- MMC/SD memory card connector
- JTAG
- 64 pin expansion connector, all LPC2148 I/O pins are available on connector
- 2.1 mm power supply connector.

Power supply:

- 9-15 VDC, ≥200 mA from 2.1 mm power connector.
- Can also be powered directly from any of mini-B USB connectors.

1.6 Registers:

ARM7 Microcontroller consists of 37 Registers. All are 32-bit in length. Out of 37 Registers 30 are General purpose Registers, six are status Registers and one is a program counter

1.8 Memory Architecture: There are two types of memory systems are used firstly On-chip flash memory system is LPC2148 incorporate a 512 kB Flash memory system. This memory may be used for both code and data storage. When the LPC2148 on-chip boot loader is used, 500 kB of Flash memory is available for user code. The LPC2148 Flash memory provides minimum of 100,000 erase/write cycles and 20 years of data-retention. Secondly On-chip Static RAM (SRAM) may be used for code and/or data storage. The on-chip SRAM may be accessed as 8- bits, 16-bits, and 32-bits. The LPC2148 provide 32 kB of static RAM. The LPC2148 SRAM is designed to be accessed as a byte-addressed memory.

2. MATERIALS, METHODS AND DISCUSSION

2.1 DTMF (Dual Tone Multiple Frequency):

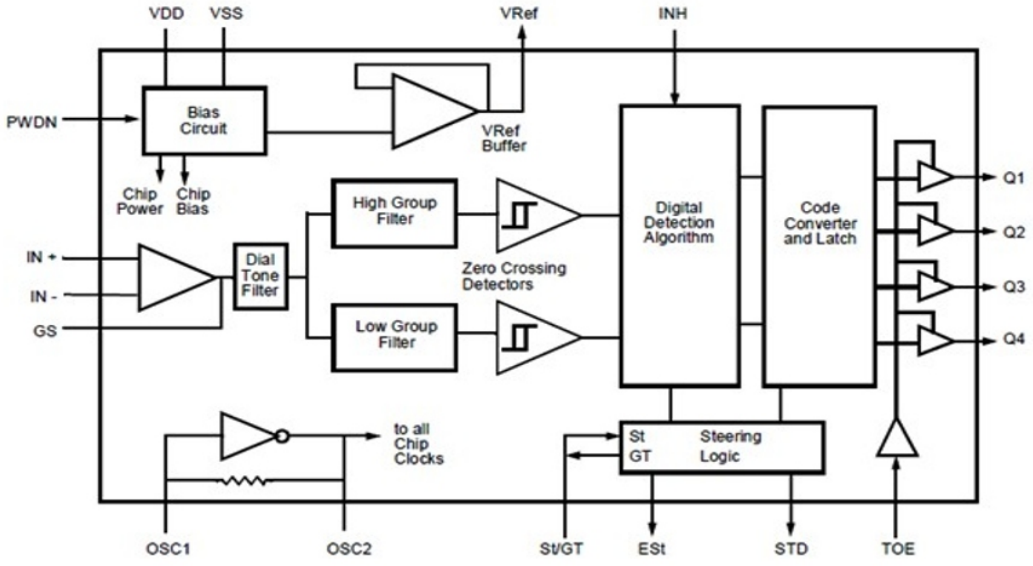


Fig 2.1: DTMF Block Diagram

Filter Section:

Separation of the low-group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor band pass filters, the bandwidths of which correspond to the low and high group frequencies. The filter output is followed by a single order switched capacitor filter section which smoothes the signals Prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals.

Decoder Section:

Digital counting techniques to determine the frequencies of the incoming tones and to ve- rify that they correspond to standard DTMF frequencies. When the detector recognizes the pres- ence of two valid tones the "Early Steering" (ESt) output will go to an active state. Any subse- quent loss of signal condition will cause ESt to assume an inactive state.

Steering Circuit:

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. The steering circuit works in reverse to validate the inter digit pause be- tween signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (dropout) too short to be considered a valid pause. This facility, to- gether with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Crystal Oscillator:

The internal clock circuit is completed with the addition of an external 3.579545 MHZ crystal

Differential Input Configuration:

The input arrangement of the MT8870D/MT8870D-1 provides a differential-input opera- tional amplifier as well as a bias source (VRef) which is used to bias the inputs at mid-rail. Pro- vision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. The op-amp connected for unity gain and Vref biasing the input at 1/2VDD.

Power-down Mode:

Logic high applied to pin 6 (PWDN) will power down the device to minimize the power consumption in a standby mode. It stops the oscillator and the functions of the filters.

Inhibit Mode:

Inhibit mode is enabled by a logic high input to the pin 5 (INH). It inhibits the detection of tones.

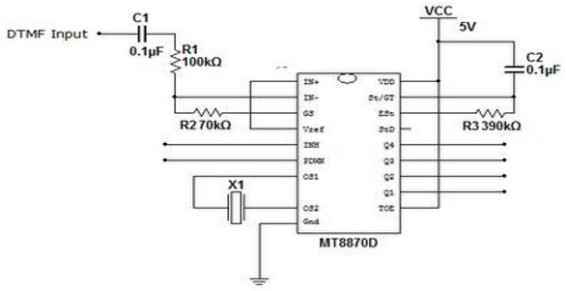


Fig 2.2: Inhibit Mode

DTMF data output table:

Low Group	H	Digit	Vt	D	D	D1	D0
	1209	1	H	L	L	L	H
697	1336	2	H	L	L	H	L
697	1477	3	H	L	L	H	H
770	1209	4	H	L	H	L	L
770	1336	5	H	L	H	L	H
770	1477	6	H	L	H	H	L
852	1209	7	H	L	H	H	H
852	1336	8	H	H	L	L	L
852	1477	9	H	H	L	L	H
941	1336	0	H	H	L	H	L
941	1209	*	H	H	L	H	H
941	1477	#	H	H	H	L	L
697	1633	A	H	H	L	H	H
770	1633	B	H	H	H	H	L
852	1633	C	H	H	H	H	H
941	1633	D	H	L	L	L	L
		ANY	L	Z	Z	Z	Z

2.2 A DC motor is designed to run on DC electric power. Types are used as brushed and brush- less types, which use internal and external commutation respectively to create an oscillating AC current from the DC source.

2.3 L293, L293D (QUADRUPLE HALF H-DRIVERS)

The L293 and L293D are used as a quadruple high-current half-H drivers. The L293 is designed to provide bidirectional drive currents of up to 1 A at voltages from 4.5 V to 36 V. The L293D is designed to provide bidirectional drive currents of up to 600-mA at voltages from 4.5 V to 36 V. Both devices are designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply ap- plications. All inputs are TTL compatible. Each output is a complete totem-pole drive circuit, with a Darlington transistor sink and a pseudo-Darlington source. Drivers are enabled in pairs, with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled, and their outputs

are active and in phase with their inputs. When the enable input is low, those drivers are disabled, and their outputs are off and in the high-impedance state. With the proper data inputs, each pair of drivers forms a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

Features:

- Featuring Unitrode L293 and L293D
- Wide Supply-Voltage Range: 4.5 V to 36 V
- Separate Input-Logic Supply
- Internal ESD Protection
- Thermal Shutdown
- High-Noise-Immunity Inputs
- Functionally Similar to SGS L293

SGS L293D

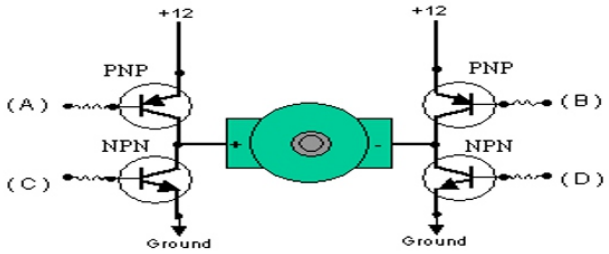
Output Current 1 A Per Channel - (600 mA for L293D)

Peak Output Current 2 A Per Channel - (1.2 A for L293D)

Output Clamp Diodes for Inductive - Transient Suppression (L293D)

2.4 H-BRIDGE:

We can better control our motor by using transistors or Field Effect Transistors (FETs). Fig 2.5 showing the solid state circuits provide power and ground connections to the motor, as did the relay circuits. The high side drivers need to be current "sources" which is what PNP transistors and P-channel FETs are good at. The low side drivers need to be current "sinks" which is what NPN transistors and N-channel FETs are good at.



A	B	C	D	Function
-	-	-	-	----------
1	0	0	1	Forward
0	1	1	0	Reverse
1	1	0	0	Brake
0	0	1	1	Brake
1	0	1	0	Fuse test :-)
0	1	0	1	Fuse test :-)

Don't do the fuse tests

Fig 2.3: H-Bridge operation

If you turn on the two upper circuits, the motor resists turning, so you effectively have a breaking mechanism. The same is true if you turn on both of the lower circuits. This is because the motor is a generator and when it turns it generates a voltage. If the terminals of the motor are connected (shorted), then the voltage generated counteracts the motors freedom to turn. It is as if you are applying a similar but opposite voltage to the one generated by the motor being turned. Vis-ã-vis, it acts like a brake.

H-Bridges Devices: The L293D has 2H-Bridges, can provide about 1A to each and occasional peak loads to 2A. Motors typically controlled with this controller are near the size ofa 35 mm film plastic canister. The L298 has 2 h-bridges on board, can handle 1A and peak current draws to about 3A. You often see motors between the size a of 35 mm film plastic canister and a coke can, driven by this type H-Bridge. The LMD18200 has one h-bridge on board, can handle about 2 or 3 amps and can handle a peak of about 6 amps. This H-Bridge chip can usually handle an average motor about the size of a coke. That's the basics about motors and H-Bridges. Hope it helps and be safe. But in our project we are using only semiconductor H- bridge i.e. using four transistors.

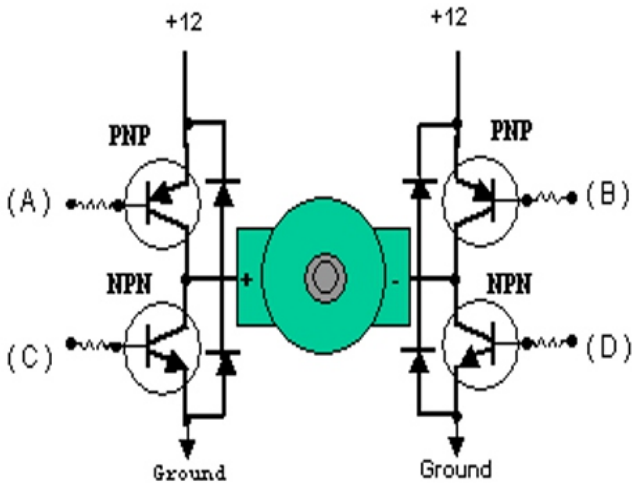


Fig 2.4: H-Bridge operation

2.5 MT8870 (INTEGRATED DTMF RECEIVER)

The MT8870D/MT8870D-1 monolithic DTMF receiver offers small size, low power consump- tion and high performance. It is a complete DTMF (Dual Tone Multiple Frequency) receiver in- tegrating both the band split filter and digital decoder functions. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code. External component count is mi- nimized by on chip provision of a differential input amplifier, clock oscillator and latched three- state bus interface.

Features:

- Complete DTMF Receiver
- Low power consumption

- Internal gain setting amplifier
- Adjustable guard time
- Central office quality
- Power-down mode
- Inhibit mode
- Backward compatible with MT8870C/MT8870C-1

2.6 ULN 2003 was used as high-voltage, high-current Darlington driver comprised of seven NPN Darlington pairs. Ideally suited for interfacing between low-level logic circuitry and multiple peripheral power loads. The ULN2003A/L have series input resisters selected for operation directly with 5V TTL or CMOS. The ULN2003 A/L are the standard Darling- ton arrays. The outputs are capable of sinking 500mA and will with stand at least 50V in the OFF state. Outputs may be paralleled for higher load current capability. The Darlington arrays are furnished in 16-pin Dual-in-line plastic package and 16-lead sur- face- mountable SOIC‟s. All devices are rated for operation over the temperature range of -20˚ C to 85˚ C.

2.7 RELAYS

A relay is used as an electrical switch that opens and closes under the control of another electrical circuit. In the original form, the switch is operated by an electromagnet to open or close one or many sets of contacts. A relay is able to control an output circuit of higher power than the input circuit, it can be considered to be, in a broad sense, a form of a electrical amplifier.

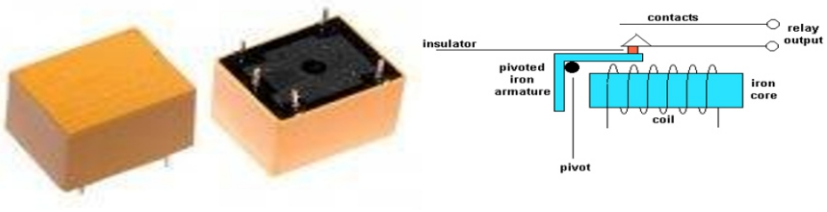


Fig2.5: Relay

Relays are usually SPDT (single pole double through switch) or DPDT (double pole double through switch) but they can have many more sets of switch contacts, for example relays with 4 sets of changeover contacts are readily available.

2.8 Basic operation of a relay:

An electric current through a conductor will produce a magnetic field at right angles to the direction of electron flow. If that conductor is wrapped into a coil shape, the magnetic field produced will be oriented along the length of the coil. The greater the current, the greater the strength of the magnetic field, all other factors being equal.

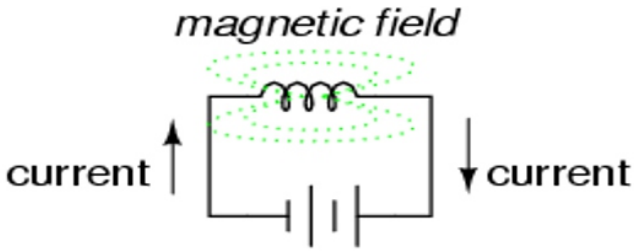
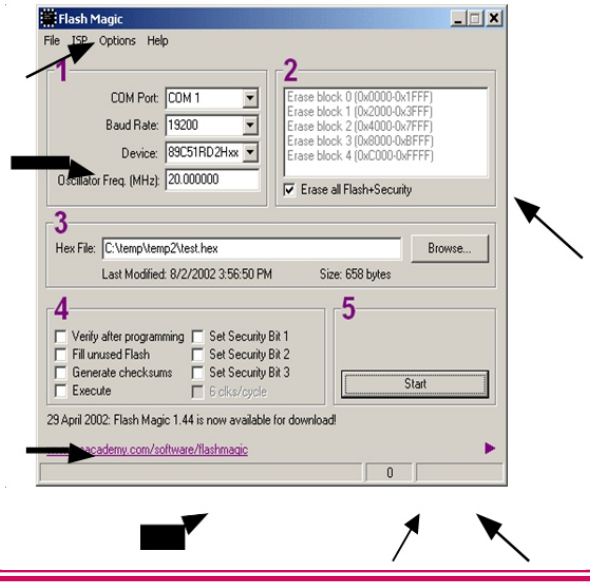


Fig 2. 6 : Basic Operation of Relay

Inductors react against changes in current because of the energy stored in this magnetic field. When we construct a transformer from two inductor coils around a common iron core, we use this field to transfer energy from one coil to the other. However, there are simpler and more direct uses for electromagnetic fields than the applications we've seen with inductors and transformers. The magnetic field produced by a coil of current-carrying wire can be used to exert a mechanical force on any magnetic object, just as we can use a permanent magnet to attract magnetic objects, except that this magnet (formed by the coil) can be turned on or off by switching the current on or off through the coil. If we place a magnetic object near such a coil for the purpose of making that object move when we energize the coil with electric current, we have what is called a solenoid. The movable magnetic object is called an armature, and most armatures can be moved with either direct current (DC) or alternating current (AC) energizing the coil. The polarity of the magnetic field is irrelevant for the purpose of attracting an iron armature. Solenoids can be used to electrically open door latches, open or shut valves, move robotic limbs, and even actuate electric switch mechanisms and is used to actuate a set of switch contacts

2.9 In This Project a Water Pump Motor is used as an DC motor which is used for pumping paint to the wall. In the synchronous motor, which does not rely on induction and as a result can rotate exactly at the supply frequency or a sub-multiple of the supply frequency and stepper motor is used as an brushless AC synchronous electric motor that can divide a full rotation into a large number of steps. The motor's position can be controlled precisely, without any feedback mechanism (see open loop control).



3. SOFTWARE REQUIREMENTS

In our project we mainly used softwares they are Keil software, Flash Magic and Proload. In Keil compiler is a software used where the machine language code is written and compiled. After compilation, the machine source code is converted into hex code which is to be dumped into the microcontroller for further processing. Keil compiler also supports C language code. Keil can be used to create source files, automatically compile, link and convert using option set. The simulator /debugger in KEIL can perform a very detailed simulation of a microcontroller along with external signals. Keil compiler is a software used where the machine language code is written and compiled. After compilation, the machine source code is converted into hex code which is to be dumped into the microcontroller for further processing. Keil compiler also supports C language code.

Minimum requirements:

Windows95/98/ME/NT, Mouse, COM Port, 16MbRAM, 3MbDiskSpace

Main Window:

The following is a screenshot of the main Flash Magic window. The appearance may differs lightly depending on the device selected.

Five Step Programming:

Step 1 – Connection Settings: Before the device can be used the settings required to make a connection must be specified. Select the desired COM port from the drop down list or type the desired COM port directly into the box. If you enter the COM port yourself then you must enter it in. Any other format will generate an error. So if you want to use COM 5 (which is not present on the drop down list) you can directly type in either “COM 5” or “5”.Select the baud rate to connect at. Try a low speed first. The maximum speed that can be used depends on the crystal frequency on your hardware. You can try connecting at higher and higher speeds until connections fail. Then you have found the highest baud rate to connect at. Alternatively, some devices support high speed communications. Select the interface being used, if any. An interface is a device that connects between your PC and the target hardware. Do not round the frequency, instead enter it as precisely as possible. Once the options are set ensure the device is running the on-chip Bootloader if you are using a manual ISP entry method. Note that the connection settings affect all ISP features provided by Flash Magic.

Menus Section 1

Section 2

Embedded Hints

Progress Information

Programmed Count

Progress bar

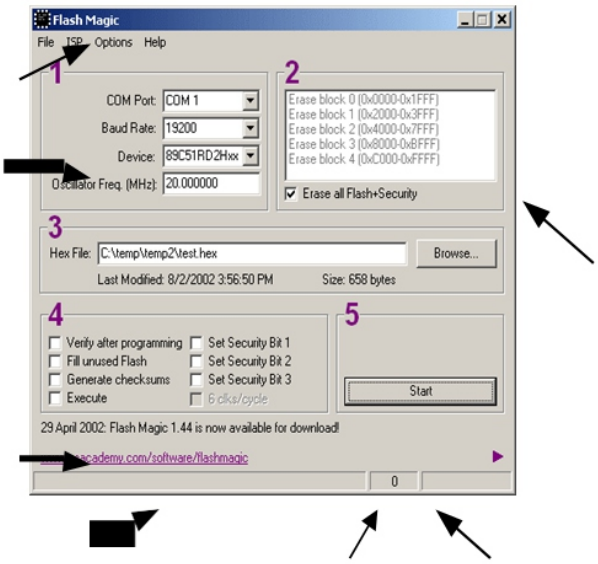


Fig 3.1: Main Window

Step 2 – Erasing:

This step is optional, however if you attempt to program the device without first erasing atleast one Flash block, then Flash Magic will warn you and ask you if you are sure you want to program the device. Select each Flash block that you wish to erase by clicking on its name. If you wish to erase all the Flash then check that option. If you check to erase a Flash block and allthe Flash then the Flash block will not be individually erased. If you wish to erase only the Flash blocks used by the hex file you are going to select, then check that option. Only when program- ming a Hex File has been completed will the Status Byte be set to 00H to allow the code to ex- ecute. This will be indicated by the text next to the Erase all Flash option. Flash will also erase the speed setting of the device (the number of clocks per cycle) setting it back to the default. This will be indicated by the text next to the Erase all Flash option.

Step 3 – Selecting the Hex File:

This step is optional. If you do not wish to program a Hex File then do not select one. You can either enter a path name in the text box or click on the Browse button to select a Hex File by browsing to it. Also you can choose Open… from the File menu. The information in- cludes the range of Flash memory used by the Hex file, the number of bytes of Flash memory used and the percentage of the currently selected device that will be filled by programming the Hex file.

If the device supports programming and execution from RAM, for example the ARM devices, then the hex file may contain records for the RAM. First the flash will be program followed by the RAM. Programs loaded into RAM via a hex file may be executed using such features as the Go option.

Step 4 – Options:

Flash Magic provides various options that may be used after the Hex File has been pro- grammed. This

section is optional, however Verify After Programming, Fill Unused Flash and Gen Block Checksums may only be used if a Hex File is selected (and therefore being pro- grammed), as they all need to know either the Hex File contents or memory locations used by the Hex File. Checking the Verify After Programming option will result in the data contained in the Hex File being read back from Flash and compared with the Hex File after programming. This helps to ensure that the Hex File was correctly programmed.

Step 5 – Performing the Operations:

Step 5 contains a Start button.

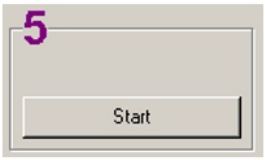


Fig 3.2 start button

Clicking the Start button will result in all the selected operations in the main window taking place. They will be in order:

- Programming the Hex File
- Erasing Flash
- Verifying the Hex File
- Filling Unused Flash
- Generating Checksums
- Programming the clocks bit
- Programming the Security Bits
- Executing the firmware

4. RESULT

The robot is controlled by mobile i.e.,[DTMF] technology, the mobile is attached to the robot when call to that phone automatically call lift when „2“ pressed it will go forward ,“8“ pressed it will move backward, „4“ pressed it will move left, „6“ pressed it will move right side, and „5“ pressed the robot will be stopped. as shown in fig.4.1

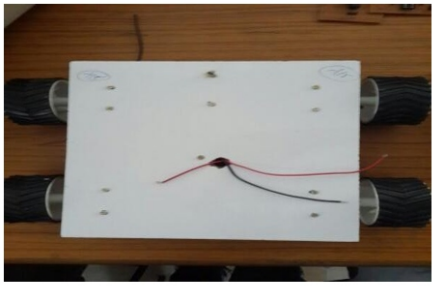


Fig 4.1 Initial stage of the project

The robot arms will be developed and then it will be move up and down the arms it will controlled by the microcontroller. The water pump will be used in the project to pump the water / paint it also controlled by the mobile. When „7“ pressed it will pump the motor and when“9“ pressed it will stop the pump. As shown in fig. 4.2

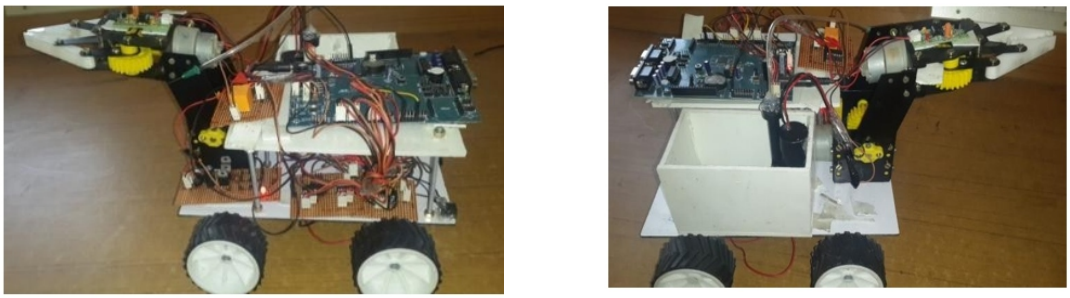


Fig 4.2: Overall View of the Project

5. CONCLUSION

Automatically paint the wall controlled by mobile [DTMF] technology has been designed and implemented in this project. The microcontroller unit to control the movement of the dc motor and spraying. The robot eliminates the hazards caused due to the painting chemicals to the human painters such as eye and respiratory system problems and also the nature of painting procedure that requires repeated work and hand rising makes it boring, time and effort consuming. The robot reduces work force for human workers and reduces time consumption. Our aim of the project to impress our objects like buildings and automobiles.

6. FUTURE SCOPE

In the future the painting robot can be enhanced by using image processing in order to scan the objectives and obstacles that are present in the wall so that those objects can be automatically omitted while painting. By keeping wireless camera in the robot we can see the painting objects clearly in the office itself.

REFERENCES

[1]. Mohamed T.Sorour, Mohamed A. Abdellatif, Ahmed. A. Ramadan, and Ahmed A. Abo- Ismail, Development of Roller Based Interior wall painting robot, world Academy of Science, Engineering and Technology Vol.59-2011.

[2]. S.M.S. Elattar, Automation and robotics in construction, opportunities and challenges, Emirates journal for engineering research, Vol.No.13 (2). Page No: 21-26-2008

[3]. Naticchia, A. Giretti, A. Carbonari, set up of a robotized system for interior wall painting, proceedings of 23rd ISARC, October 3-5,Tokyo, Japan,2006

[4]. Johan Forsberg Roger AarenstrupAke Wernersson, A construction Robot for Autonomous Plastering of walls and ceilings, Vol 6, 2000

[5]. Jayshree sahu, S.K. Sahu, Jayendra Kumar, Microcontroller Based DC Motor Control, International Journal of Engineering Research & Technology , Vol.1 Issue 3,May-2012.

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