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Contents

Mathematical Estimation of Avalanche Breakdown Voltage Equation in Vertical DIMOSFET With Gaussian Doping Profile On 4H- SIC Wafer

Parag Parashar
Department of Electronics and Communication,
Amity University Gurgaon, Haryana, India

ABSTRACT

The present work aims at the mathematical analysis and estimation of avalanche breakdown voltage equation for a Gaussian doping profile in the drift region of Vertical DIMOSFET with 4H- SiC wafer. With the help of ionization integral equation for avalanche breakdown condition, an equation has been derived that will provide values of depletion width needed for avalanche breakdown in this device. With these real depletion width values and selection of device height 'h', function constant 'm' and peak concentration ' 0' avalanche breakdown voltages can be estimated.

Keywords- Avalanche breakdown voltage, DIMOSFET, Gaussian profile, Impact ionization coefficient, Silicon, Silicon Carbide

INTRODUCTION

Silicon carbide (SiC) is a potential compound semiconductor for high temperature, frequency, and power electronic applications. It is mainly due of its wide energy band gap, high saturated drift velocity, high breakdown electric field and high thermal conductivity. There are different polytyes of SiC with stacking order between the double layers of carbon and silicon atoms define the difference. The most important polytypes are hexagonal 4H, 6H and cubic 3C-SiCform. The distinct polytypes differ in both band gap energies and electronic properties. Thus band gap varies with the polytype from 2.2eV for 3C-SiC over 3.0eV for 6H-SiC to 3.2eV for 4H-SiC. The development of SiC devices has been mainly based on 4H– SiC which compared to other polytypes has a wider band gap, higher mobility and higher breakdown voltage. The electron mobility of 4H- SiC is almost twice or 10 times that of 6H- SiC in the direction perpendicular to or along the 6H-SiC c-axis. 4H-SiC devices have lower specific on-resistance with respect to other semiconductors such as Si, GaAs and 6H- SiC[1]. But due to different types of defects such as micropipes, etch pits, super dislocations, planer improvements in crystal growth and device fabrication processes are needed before SiC- based devices and circuits can be scaled-up and reliably incorporated into electronic systems. However, a lot of work is being done in reduction of structural defects, deep level defects, point defects, and carrier lifetime improvement of thick epitaxial layers of 4H- SiC [2-4] .For high power application, calculation of breakdown voltage is an important parameter. There is an unprecedented growth in this area and in recent years breakdown voltage in the

range of 12kV has been achieved for IGBTs and the value stand near 20kV for PIN diodes [5-6]. A mathematical analysis has been done in this paper to derive equation for avalanche breakdown voltage for Gaussian doping profile in the drift region of DIMOSFET for 4H SiC wafer.

THEORY

The fabrication of vertical DIMOSFET structure is normally done by using planar diffusion technology with a gate such as poly silicon. In these devices, poly silicon gate edge works as a common window for the implantation of p-base and n+ - source regions. Figure 1 represents a cross section of a DIMOSFET structure. Difference in the lateral diffusion between the p-base and n+ source region defines the surface channel region [7]. The forward blocking capability is achieved by the p-n junction between the p-base region and low doped n-drift region. During the device operation, a fixed potential to the p-base region is provided by the connection of base to the source metal through a break in the n+ source region. By applying a positive bias to the drain and short-circuiting the gate to the source, the p-base and n-drift region junction becomes reverse-biased thus supporting the drain voltage by the extension of a depletion layer on both sides of the junction [7]. However, the depletion layer extends primarily into the n-drift region due to its lower doping level as compared to p-base region. A conductive path extending between the n+ - source region and the n-drift region is formed by applying positive bias to the gate electrode. The application of a positive drain voltage results in a current flow between drain and source through the n-drift region and conductive channel.

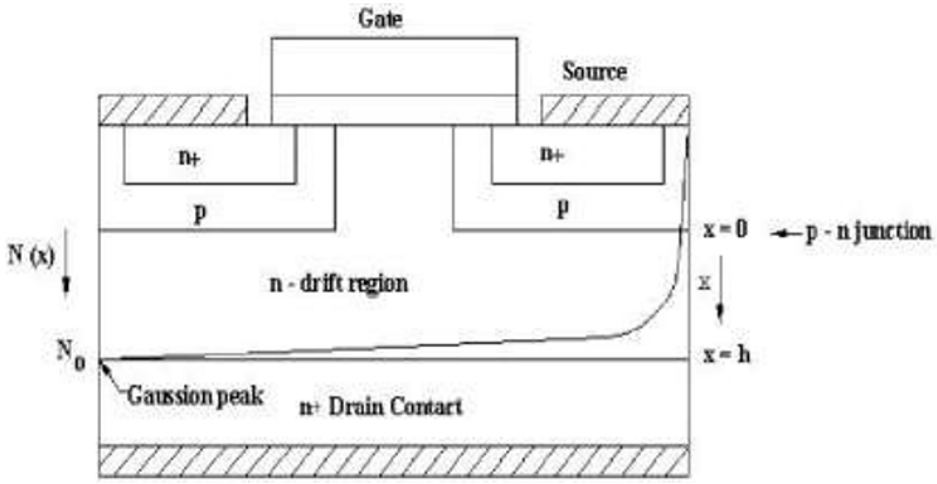

Figure 1.Cross Sectional Structure of DIMOSFET Showing Gaussian Profile in the Drift Region [8]

Doping profiles used in semiconductor industry commercially normally have non-linearly graded profiles inside semiconductor layers. These profiles usually adopt Gaussian, Complementary Error Function distribution or an exponential distribution for improved results [8]. In this paper analysis of Gaussian profile has been adopted with the peak lying at the drain end of the device and the doping concentration falls to small values near the n-drift region and p-base junction. Thus enabling, a low

parasitic series resistance near the drain and a large depletion region in the drift region near the junction.

The impact ionization coefficient for a charge carrier is defined as the number of electron– hole pairs created by a charge carrier traversing 1 cm through the depletion layer along the direction of the electric field. Infinite impact ionization rate has been defined as the condition for avalanche breakdown [9]. To analyze this, consider a one-dimensional reverse-biased N+ P junction with a depletion region extending mainly in the P-region. If an electron–hole pair is generated at a distance x from the junction, the electron will move towards the junction to the N+ -region, while the hole will simultaneously move towards the contact of P-region. These charge carriers under the influence of large electric field in the depletion region will be accelerated until they gain sufficient energy to create electron–hole pairs during collisions with the lattice atoms. Based upon the definitions for the impact ionization coefficients, the hole and the electron will create [α_n dx] and [α_p dx] electron–hole pairs when traversing a distance dx through the depletion region, respectively. Here, α_n and α_p are the impact ionization coefficients for electrons and holes respectively. Due to a single electron–hole pair initially generated at a distance x from the junction, the total number of electron–hole pairs created in the depletion region is given by [9]

$$M(x) = 1 + \int_0^x \alpha_n M(x)dx + \int_x^W \alpha_p M(x)\,dx \quad (1)$$

where ,W is the width of depletion region. A solution for this equation is given by [9]

$$M(x) = M(0) \exp\left[\int_0^x (\alpha_n - \alpha_p)\,dx\right] \quad (2)$$

Where M (0) represents the total number of electron–hole pairs at the edge of the depletion region. Putting this expression in (1) with $x = 0$ provides a solution for M (0) [9]

$$M(0) = \left\{1 - \int_0^W \alpha_p \exp\left[\int_0^x (\alpha_n - \alpha_p)\,dx\right] dx\right\}^{-1} \quad (3)$$

By putting above expression in equation (1), we have [9]

$$M(x) = \frac{\exp\left[\int_0^x (\alpha_n - \alpha_p)\,dx\right]}{1 - \int_0^W \alpha_p \exp\left[\int_0^x (\alpha_n - \alpha_p)\,dx\right] dx} \quad (4)$$

If the electric field distribution along the impact ionization path is known, then above expression for $M(x)$, which is known as the multiplication coefficient results in calculation of the total number of electron–holes pairs created as a result of the generation of a single electron–hole pair at a distance x from the junction. For avalanche breakdown condition, M should be equal to infinity. This condition is obtained by putting the denominator of equation (4) equal to zero [9]

$$\int_0^W \alpha_p \exp\left[\int_0^x (\alpha_n - \alpha_p)\,dx\right] dx = 1 \quad (5)$$

Left-hand side expression is known as the ionization integral. For the analysis of avalanche breakdown in power devices, a voltage at which the ionization integral becomes equal to unity is found out. If the impact ionization coefficients for electrons and holes are supposed to be equal, the avalanche breakdown condition reduces to [9]

$$\int_0^W \alpha \, dx = 1 \tag{6}$$

Equation (6) has been used in the present work for the estimation of avalanche breakdown voltage. This method of determination of the breakdown voltage is valid for power rectifiers and MOSFETs where the current flowing through the depletion region is not amplified [9].

Result and Calculations

Baliga's power law approximation for the impact ionization coefficients for 4H-SiC for analytical derivations is given as [9]

$$\alpha = 3.9 \times 10^{-42} E^7 \tag{7}$$

where, E is the electric field distribution.

The equation for Gaussian profile is written as [7]

$$G(x) = N_0 \, exp^{-\frac{h-x^2}{m}} \tag{8}$$

N_0 is the maximum concentration at the drain end, 'h' is device height, m is a function constant. The depletion region width at any given reverse voltage V can be obtained by solving the Poisson's equation for the system.

For the Gaussian function G(x), the Poisson's equation becomes [7]

$$-\partial^2 V/\partial^2 x = \frac{N_0}{\varepsilon_s} exp^{-\frac{h-x^2}{m}} \tag{9}$$

ε_s is the relative permittivity of medium and e is the charge of an electron.

Integrating equation (9) from 0 to x will give electric field E as [7]

$$E = \frac{-\sqrt{\pi}\, e N_0 m}{2\varepsilon_s} \operatorname{erf}\frac{hx}{m} + C \tag{10}$$

At x=h, E=0 therefore C=0. So, equation becomes [7]

$$E = \frac{-\sqrt{\pi}\, e N_0 m}{2\varepsilon_s} \operatorname{erf}\frac{h-x}{m} \tag{11}$$

Integrating the above equation for voltage V with proper initial conditions and first order error function approximation, we get [7]

$$\frac{W^4}{12m^2} - \frac{hW^3}{3m^2} - \frac{W^2}{2}\left(1-\frac{h^2}{m^2}\right) - \frac{\varepsilon_s V}{e N_0} = 0 \tag{12}$$

Above equation will be used to estimate avalanche breakdown voltage V_a(by replacing V) at a particular depletion width 'W'.

Putting equations (7) and (11) in equation (6), we have

$$\int_0^W 3.9\times10^{-42}\left[\frac{-\pi e N_0 m}{2\varepsilon_s}\right] \text{erf}\left[\frac{h-x}{m}\right] dx = 1 \quad (13)$$

$$3.9\times10^{-42}\left(\frac{-\pi e N_0 m}{2\varepsilon_s}\right)^7 \int_0^W erf\left(\frac{h-x}{m}\right)^7 dx = 1 \quad (14)$$

For $\frac{h-x}{m} < 1$, error function can be expressed as:

$$\text{erf}\left(\frac{h-x}{m}\right) = \frac{2}{\sqrt{\pi}}\left[\frac{h-x}{m} - \frac{2}{3}\left(\frac{h-x}{m}\right)^3 + \frac{1}{5}\left(\frac{h-x}{m}\right)^5 - \frac{1}{21}\left(\frac{h-x}{m}\right)^7 + \frac{1}{108}\left(\frac{h-x}{m}\right)^9 + \ldots\ldots\right]$$

Substituting above expression in equation (14) and retaining the first five terms

$$3.9\times10^{-42}\left(\frac{-\pi e N_0 m}{2\varepsilon_s}\right)^7 \int_0^W \left[\frac{2}{\sqrt{\pi}}\left(\frac{h-x}{m}\right) - \frac{2}{3}\left(\frac{h-x}{m}\right)^3 + \frac{1}{5}\left(\frac{h-x}{m}\right)^5 - \frac{1}{21}\left(\frac{h-x}{m}\right)^7 + \frac{1}{108}\left(\frac{h-x}{m}\right)^9\right]^7 dx = 1 \quad (15)$$

Solving above equation and retaining first two terms in integration, we have

$$3.9\times10^{-42}\left(\frac{-\pi e N_0 m}{2\varepsilon_s}\right)^7 \int_0^W \left[\frac{128}{\pi^7 2 m}\left(\frac{h-x}{\ }\right)^7 - \frac{896}{3\pi^7 2 m}\left(\frac{h-x}{\ }\right)^9\right] dx = 1 \quad (16)$$

Solving above equation, we have

$$3.9\times10^{-42}\left(\frac{-\pi e N_0 m}{2\varepsilon_s}\right)^7 \left[\frac{128(-7h^9+3h^7m^2)W}{3m^9\pi^7 2} - \frac{448(-3h^8+h^6m^2)W^2}{m^9\pi^7 2} + \frac{896(-4h^7+h^5m^2)W^3}{m^9\pi^7 2} + \frac{224(28h^6-5h^4m^2)W^4}{m^9\pi^7 2} + \frac{896(-42h^5+5h^3m^2)W^5}{5m^9\pi^7 2} - \frac{448(-14h^4+h^2m^2)W^6}{m^9\pi^7 2} + \frac{128(-28h^3+hm^2)W^7}{m^9\pi^7 2} - \frac{16(-84h^2+m^2)W^8}{m^9\pi^7 2} - \frac{896hW^9}{3(m^9\pi^7 2)} + \frac{448W^{10}}{15m^9\pi^7 2}\right] = 1 \quad (17)$$

Equation (17) will be solved for real values of depletion width W <h. For that depletion width avalanche breakdown condition is applicable. Putting real values of W from equation (17) into equation (12) will provide the estimated avalanche breakdown voltages V_a for a device height 'h', function constant m and peak concentration N_0.

CONCLUSION

Ionization integral condition for avalanche breakdown voltage has been used for the derivation of a mathematical equation for a Vertical Double implanted Metal oxide field effect transistor with Gaussian doping profile in the drift region for 4H- SiC wafer. Equation (17) will be solved for getting real values of depletion width less than the device height (W<h). These real values of depletion region width can be put into equation (12) for the estimation of avalanche breakdown voltages V_a for a device height 'h', function constant 'm' and peak concentration N0.

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Bridgeless Sepic Power Factor Correction Rectifier

Soumya Ramanath[1], Nimmy George[2]
[1]PG Scholar, Electrical and Electronics dept, SNGCE, India.
[2]Assistant professor, Electrical and Electronics dept, SNGCE, India.

ABSTRACT

In this paper, the Single Ended Primary Inductor converter (SEPIC) is used to achieve high power factor with reduced input current ripple. The conventional power factor correction suffers from high conduction losses due to the diode bridge at the input side. Thus bridgeless SEPIC converter is used to avoid conduction loss by using only two semiconductor switches in the current flowing path during each switching cycle. By implementing the improved topology in DCM it ensures almost unity power factor in a simple and effective manner.

Keywords- Discontinuous Conduction Mode (DCM), Power Factor Correction (PFC), Single Ended Primary Inductance Converter (SEPIC).

1. INTRODUCTION

SEPIC is a DC/DC converter topology that provides a positive regulated output voltage from an input voltage that varies from above to below the output voltage. This type of conversion is simple when the designer uses voltages from an unregulated input power supply. Hence this is very much preferred in applications such as battery chargers, power electronic circuits, home appliances, aircraft due to its less electromagnetic interference, inherent inrush current, reduced noise disturbances and less switching losses. The SEPIC topology is difficult to understand and requires two inductors, making the power-supply quite large.

Most of the presented bridgeless topologies so far [1]–[9] implement a boost-type circuit configuration (also referred to as dual-boost PFC rectifiers) because of its low cost and its high performance in terms of efficiency, power factor, and simplicity. These features have led power supply companies to start looking for bridgeless PFC circuit topologies. In [7], a systematicreview of the bridgeless PFC boost rectifier implementations that have received the most attention is presented along with their performance comparison with the conventional PFC boost rectifier. The bridgeless boost rectifier has the same major practical drawbacks as the conventional boost converter, such that the dc output voltage is always higher than the peak input voltage, input–output isolation cannot easily be implemented, the starting inrush current is high, and there is a lack of current limiting during overload conditions. Moreover, it is well known that the boost converter operating in discontinuous current mode (DCM) can offer a number of advantages such as inherent PFC function, very simple control, soft turn-on of the main switch, and reduced diode reversed-recovery losses. However, the DCM operation requires a high- quality boost

inductor since it must switch extremely high peak ripple currents and voltages. As a result, a more robust input filter must be employed to suppress the high-frequency components of the pulsating input current, which increases the overall weight and cost of the rectifier. The operation of SEPIC is similar to the bridgeless buck-boost PFC converter which has only three conducting semiconductors at every moment [1]. Comparing with the cascade buck-boost CBB- PFC converter, the efficiency is increased. Power factor is more than 0.98, and total harmonic distortion (THD) is less than one. The main features of the presented converter include high efficiency, low voltage stress on the semiconductor devices, and simplicity of design. These advantages are desirable features for high-power and high-voltage applications. The study of Bridgeless SEPIC Power Factor Correction rectifier under Discontinuous Conduction Mode is presented.

2. BRIDGELESS SEPIC PFC RECTIFIER

The bridgeless PFC circuits based on SEPIC with low conduction losses, is shown in Fig 1. Unlike the boost converter, the SEPIC converters offer several advantages in PFC applications, such as easy implementation of transformer isolation, inherent inrush current limitation during start-up and overload conditions, lower input current ripple, and less electromagnetic interference (EMI) associated with the DCM topology.

The topologies in Figure 1are formed by connecting two DC–DC SEPIC Converter one for each half-line period of the input voltage The operational circuits during positive and negative half- line period for the proposed bridgeless SEPIC rectifier of Fig.1 is shown respectively. Note that,by referring to Fig.1 there are one or two semiconductors in the current flowing path. Each of the rectifier utilizes two power switches (Q1 and Q2), two low-recovery diodes (Dp and Dn), and a fast diode (Do). However, the two power switches can be driven by the same control signal, which significantly simplifies the control circuitry. Moreover, the structure of the proposed topologies utilizes one additional inductor compared to the conventional topologies, which are often described as a disadvantage in terms of size and cost. However, better thermal performance can be achieved with the two inductors compared to a single inductor. This is because each power switch is operating during half-line period. On the other hand, the components voltage stresses are equal to their counterparts in the conventional SEPIC converter.

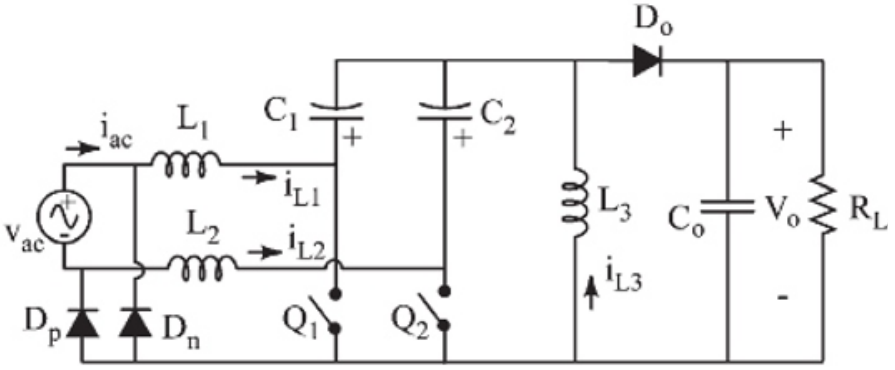

Fig1: Bridgeless SEPIC PFC Rectifier

3 . PRINCIPLE OF OPERATION OF THE BRIDGELESS RECTIFIER

The bridgeless rectifier shown in Figure 1 is constructed by connecting two DC–DC converters. Referring to Figure 1 during the positive half-line cycle, the first DC–DC SEPIC circuit L1−Q1−C1−L3−Do is active through diode Dp, which connects the input ac source to the output ground. During the negative half-line cycle, the second DC–DC SEPIC circuit, L2−Q2−C2−L3−D0, is active through diode Dn, which connects the input ac source to the output ground. Thus, due to the symmetry of the circuit, it is sufficient to analyse the circuit during the positive half-period of the input voltage. The rectifier is operated when the switch Q1 is turnedon then diode Dp is forward biased by the sum inductor currents iL1 and iL2. As a result, diode Dn is reversed biased by the input voltage. The output diode is reversed biased by the reverse voltage (Vac + V0). Thus, the loss due to the turn-on switching losses and the reverse recovery of the output diode are considerably reduced. Equations for both rectifiers are identical, provided that the voltages on the capacitors for the SEPIC rectifier.

$$V_{c1}\ t = V_{c2}\ \ t + V_{ac}\ \ t\ = \begin{matrix} V_{ac}\ t\ ; 0 \le\ t\ \le T/2 \\ 0 \qquad ; T/2\ \le\ t\ \le T \end{matrix}$$

4. MODES OF OPERATION

The circuit operation during one switching period Ts in a positive half-line period can be divided into three distinct operating modes, as shown in Fig 2 to Fig 4, and it can be described as follows.

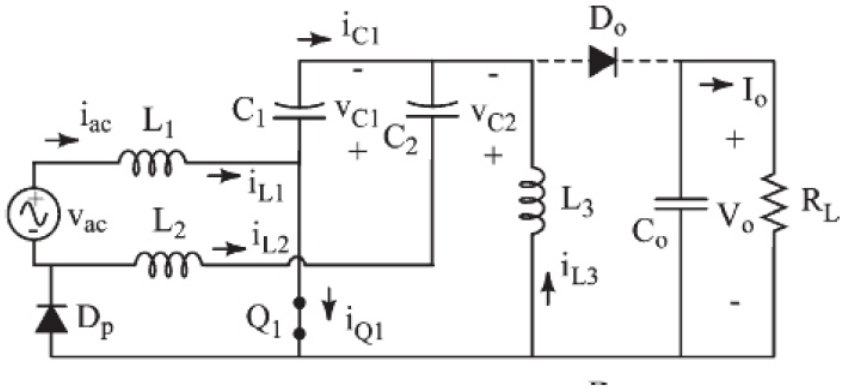

Fig 2 : Switch Q1 ON Topology

Mode 1 [t_0, t_1]

In this stage, the three-inductor currents linearly increase at a rate proportional to the input voltage *v*ac. The rate of increase of the three inductor currents is given by

$$\frac{di_{Ln}}{dt} = \frac{V_{ac}}{dt} \qquad\qquad n\ = 1,2,3$$

During this stage, the switch current is equal to the sum of the three inductors currents. Thus, the peak switch current I_{Q1-pk} is given by

$$I_{Q1-pk} = \frac{V_m}{L_g} D_1$$

where,

$$\frac{1}{L_g} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3}$$

Let D_1 be the duty cycle of switch Q_1. This interval ends when Q_1 is turned off, initiating the next subinterval.

Mode 2 [t_1, t_2]

At the instant t_1, switch Q_1 is turned off, diode Do is turned on, simultaneously providing a path for the three inductor currents. Diode D_p remains conducting to provide a path for iL_1 and iL_2. In this stage, the three inductor currents linearly decrease at a rate proportional to the output voltage V_o. The three inductor currents are given by

$$\frac{dL_n}{dt} = \frac{-V_0}{L_n} \qquad n = 1,2,3$$

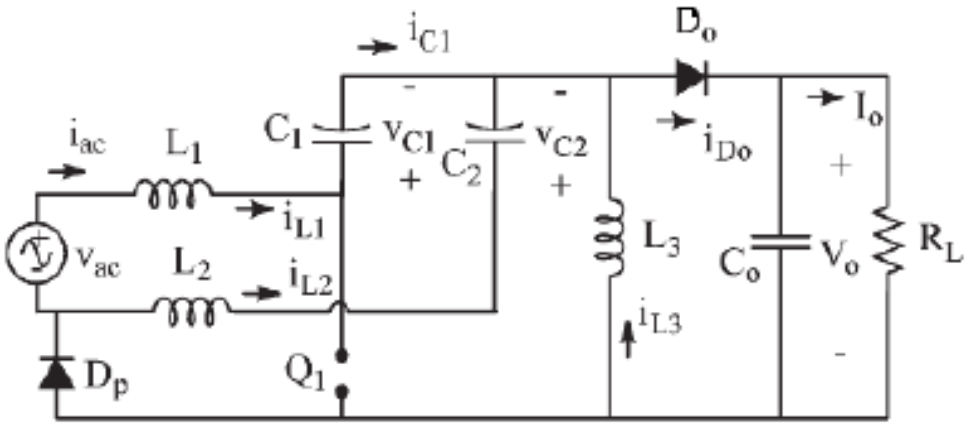

Fig 3: Switch Q1 OFF Topology

At the end of this mode the output diode current i_{DO} smoothly reaches to zero and Do becomes reverse biased. The normalized length of this interval is given by

$$D_2 = \frac{D_1}{M} sin\omega t$$

Mode 3 [t_2, t_s]

In this stage, both Q_1 and D_o are in their off-state. Diode D_p provides a path for i_{L3}. The three inductors behave as current sources, which keeps the currents constant. Hence by end of this interval, the voltage across the three inductors is zero. Capacitor C_1 is charging up by iL_1, while C_2 is discharged by i_{L2}.

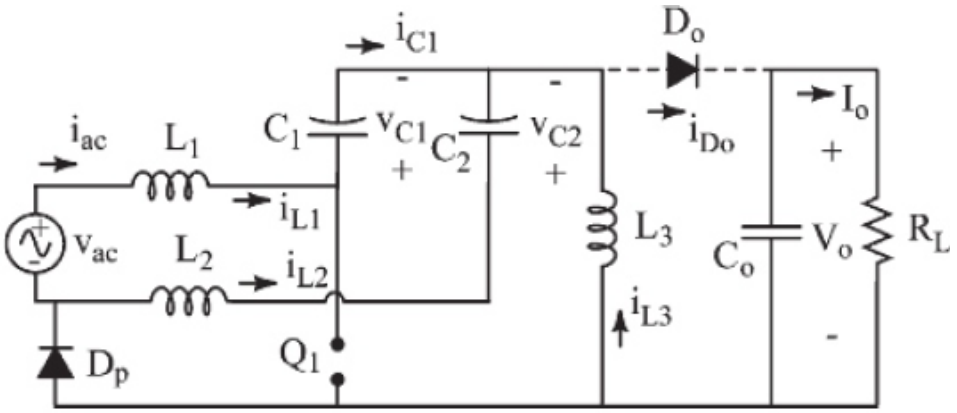

Fig 4: DCM Topology, Solid And Dashed Lines Represent Active And Inactive Elements.

5. COMPARISION BETWEEN CONVENTIONAL AND BRIDGELESS SEPIC PFC RECTIFIER

The circuit components in both the conventional PFC SEPIC rectifier and the improved bridgeless PFC SEPIC have similar peak voltage and current stresses. However, the bridgeless SEPIC is subjected to the input inductors (L1 and L2), the coupling capacitors (C1 and C2), and the active switches (Q1 and Q2) to a lower rms current stress compared to their counter parts in the conventional SEPIC topology. Moreover, the bridgeless SEPIC is constructed by connecting two DC–DC converters, each operating as SEPIC DC-DC converter, the switching performance of the two converters remains the same, which results in switching losses. Table 1 gives the comparison between conventional and bridgeless SEPIC PFC DCM based on the equipments and current conduction path.

TABLE 1: Comparison Between Conventional And Bridgeless SEPIC PFC DCM Rectifier

ITEM		Bridgeless SEPIC	conventional SEPIC
Slow diode		2	4
Fast diode		1	1
Switch		2	1
Current conduction path	Stage1	1Slow diode 1Fast diode	2Slow diodes, 1Switch
	Stage2	1Slow diode 1Fast diode	2Slow diodes 1Fast diodes
	DCM	1Slow diode	2Slow diodes

6. CONCLUSION

The single-phase bridgeless rectifiers with low input current distortion and low conduction losses have been presented. The bridgeless rectifier is derived from the conventional SEPIC converter. Comparing with conventional SEPIC and Power Factor Correction circuits, due to the lower conduction loss and switching loss, Bridgeless DCM SEPIC PFC rectifier topologies can further improve the conversion

efficiency. To maintain same efficiency, the improved circuits could operate with higher switching frequency. Thus, additional reduction in the size of PFC inductor and EMI filter could be achieved. Besides improving circuit topology and performance, a further reduction in rectifier size could be realized by integrating the three inductors into a single magnetic core.

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Distribution in Low Power Clock using Multiple Voltages and Reduced Swings

Peeyush Agarwal, Arvind S. M., Sangya Thakur, Paras Dhama,
SRM University
Kattankulathur, India.

A B S T R A C T

Significant fractions of the dissipation in power of a chip is accounted by clock networks and are critical to performance. The algorithms and theory for building a low power clock tree is presented in this paper when at a lower voltage, the clock signal is distributed and is translated to a voltage which is high at the utilization points. The low power schemes to be used are two: reduction in swing and many supply voltages. The issue of construction of tree and present conclusions which are relevant to many technology generations as per the NTRS are analyzed.

1. INTRODUCTION

One of the most important parts of a synchronous VLSI chip are constituted by the clock signal as it can influence the area, power dissipation and speed of the system.

Power dissipation is one major drawback associated with clock networks. It is shown in studies that the power dissipated by clock network is 20-50% of the total power on a chip. Strategies for significantly reduction in the power dissipation of the clock network are needed to develop ,the work in this paper is based on the observation that the clock network can be made to dissipate less power by using a lower Vdd to distribute the signal over the chip.

Research has been done on the problem of clock tree synthesis for zero skew. A recursive bottom-up combination of two zero-skew subtrees has been performed by this method by finding a tapping point which ensures zero skew in the subtree which is larger. A method called The Deferred-Merged Embedding (DME) embeds a given clock tree topology optimally in the Manhattan plane with skew of zero and attempt are made so that the total wire length is minimized.

Controlling of the short circuit dissipation of power is done by the enforcement of a constraint that the clock edge should never have a transition (rise/fall) time larger than a given specified time throughout the clock tree.

The below stated equation lists the expression for the charge/discharge power dissipation.

$P = fC_L V_{dd} V_s$ **equation 1**

Where clock frequency is f, load capacitanceis the C_L, supply voltage is the V_{dd}, and the output swing of the buffer is V_s. In the cases where the output of the buffer swings from 0 to V_{dd}, V_s and V_{dd} have the same value and the formula reduces to $P = f C_L V_{dd}^2$.

Since fundamental parameter for the circuit is f, no changes can be made and the reduction in its effects can only be done by techniques like clock gating.

Therefore, the reduction in the dissipation of power in the clock network can only be made by

(a) Reduction in the total load capacitance, that is consistent with attempting which leads in achievement in the minimal wire length and the minimal power dissipation in buffer.

(b) Reduction in V_{dd}, which leads to a quadratic reduction provided there is also simultaneous reduction in Vs by the same factor.

(c) Reduction in V_s without a reduction in V_{dd}, which is corresponding with a linear reduction in the dissipation of power.

A new theory is presented in this work and results for building low power clock trees using a smaller voltage to distribute the signal over the chip, and then converting this low voltage clock signal is done back to a higher voltage at the utilization points.

1. STATEMENT OF THE PROBLEM

1.1 Structure of the Clock Tree

A multiple supply voltages clock scheme was proposed and is illustrated in Figure 1 below.

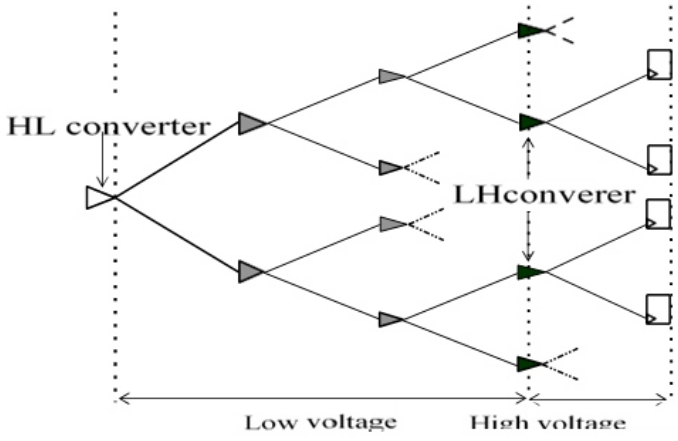

Figure 1: Low Power Clock Scheme

In order for the regeneration of the signal and maintenance of a sharp slew rate when the signal goes through the network, the use of immediate buffers is recommended in the clock tree. It is proposed in this paper, an HL converter is inserted without giving a justification that is specific, at the root of the clock tree, , and at the clock sinks, LH converters are inserted, which finally leads to the placing of the entire clock tree in the region of low voltage.

1.2 Level Converter Circuits

1.2.1 A Level Converter Using Multiple Supply Voltages

The need is to convert the clock swing from a voltage range which is high of gnd to V_{ddH} to a voltage range which is low of gnd to V_{ddL}. For ensuring that there is no transient current which is having significance, the part which V_{ddH} drives is having more usage of feedback which helps to speeding up of the transition.

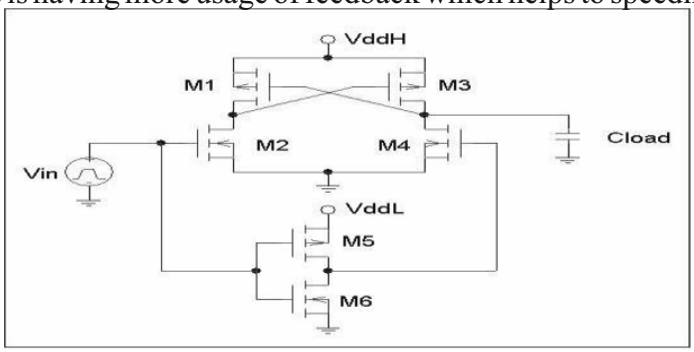

Figure 2: An LHconverter circuit

1.2.2 A Level Converter by the use of Reduced Clock Swing

Output clock swing is another variable that can be adjusted so that dissipation of power is reduced as explained in equation (1). For the problem of clock tree, there would be delay and transition times by the use of a driver to drive a long interconnecting wire without the use of any repeater drivers. A clock scheme with reduced-swing is presented with drivers in this paper, as illustrated in Figure 3. The driver having reduced swing is shown in Figure 3 and its output swings that change its value from V_{tn} to V_{dd}-$|V_{tp}|$. For acting as an inverter, M4 and M5 are there and M3 and M6 change the ground and supply voltages to V_{dd}-$|V_{tp}|$ and V_{tn}, respectively, hence ensuring a zero steady-state short circuit current and keeping both the output swing and the input swing same.

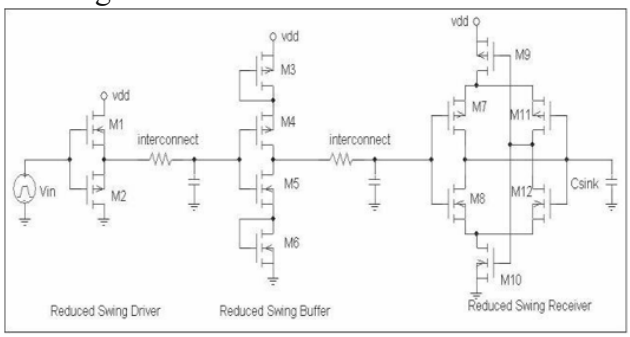

Figure 3: Clock Scheme withReduced Swing

Finally, there is a modification version of the fully complementary Self-Biased CMOS differential amplifier, the reduced spring receiver. By feeding back the output signal to the other differential input node, the modification is performed.

A few comments about the circuits above are in order:

1. The transistors will have to be sized appropriately.

2. The transistors M3 and M6which are present in the reduced swing buffer. When the output voltage reaches Vdd-|Vtp| [Vtn] makes the output swing limited by turning off a path to Vdd [ground]. Availability of discharge path is negligible to reduce the voltage back to Vdd-|Vtp| if the voltage on the connected wire rises above Vdd|Vtp| due to the reason of coupling with another wire. Unexpected skews can be brought out because of the delay in fall to increase from the nominal value.

3. The outputs of the reduced swing buffer can rise towards Vdd or fall towards ground due to the leakage currents, it is also dependent on the polarity the output state is having, if the clock is stopped for a period of time so that power can be saved. As a result, unexpected skews can be seen in the first clock cycle after the reactivation of the clock is done. By the usage of a design discipline that starts the clock one or more cycles earlier to when it is required to be started, this may be overcome.

4. The delays in the given circuits are susceptible to effects of noise and noise having power supply same as the ones described in item 3.

INSERTION OF BUFFER

The possibility of buffer insertion at the base of the twosubtrees which are child is considered after joining of each pair of sub trees. For a buffer to be inserted, the criterion is that the slew rate at each buffer input and each sink node is faster than a specified given amount.

There are two reasons that the Lhconverters are placed having a major impact on the dissipation of power of the clock tree:

(a) More numerous converters than any other type of buffer are LH converters as the converters which are at the lowest stage of the clock tree are LH converters.

(b) A larger amount of power per unit wire length is consumed by the wires downstream of the Lhconverters because they are driven at the high swing.

An important role is played in the total power dissipation of the tree by the positioning of LH converters.

1.3 Theoretical Results on Buffer Positioning

The criteria which is used to determine the results determine the positions of the LHconverters, by using a common area measure that gives an estimation of it as the sum of buffer widths.

Theorem 1: For the buffer area solution to be minimum, the insertion of LH converters is necessary at the clock sinks, appropriately sized so that the clock slew rate constraints can be met.

Proof: Let two subtreesT1 and T2 be taken that are zero-skew merged to form a subtree which is large, as it is shown in Figure 4. Two options are considered for the possibility of inserting an LHconverter in this subtree is:

(a) The subtree formed by merging T1 and T2is driven by an LH converter if size w1

(b) LHconverters of size w2 and w3,drives T1 and T2respectively

The sizes of LHconverter are chosen that requirements of edge rate for each subtree are not be met by the use of same size of LH converter.

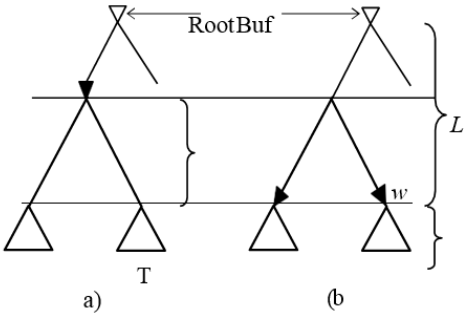

Figure 4: Buffer Placement

W_1 must be greater than w_2+w_3in order for option (b) to be an area-optimal solution.

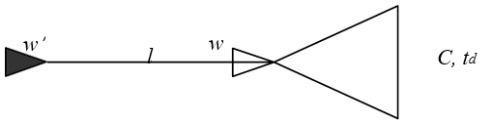

Figure 5: Buffer Sliding

A subtree driven by a buffer as shown in figure 5, of which characterization is done by the delay downstream, t_d and the capacitance downstream, C,. The relationship between w and w′ can then be given as:

$t/2=k/w`(C+lC)+r_0 l\,C+lC_0/2+t_d=(k/w)\,c+t$

Where t_d and Care, respectively, the downstream delay and capacitance of the location of buffer w, the length of the segment along which w is moved up to w' is l, and k, r_0 and C_0 are respectively, the unit resistance of buffer, the unit resistance of wire and the unit capacitance of the wire. This leads to the relation

$1/w' (1+lC/C) + r_0 l/k (1+lC/2C) = 1/w$

Since it can be clearly seen that the factor of multiplication for 1/w' is much larger than 1 and a positive number is added to the quantity, this gives us a result 1/w> 1/w', i.e., w' >w.

Therefore, when Figure 4(b) which has both the buffers are made to slide up until they are just merging point downstream, as shown in Figure 6(b) the size w2'>w2and w3' >w3.

For the transition time requirement to be satisfied at the leaf nodes, the following relationship must hold.

$K / w2' ((l_1 + l_2)C_o + C_1 + C_2) + r_o l_1 C_o l_1 + C_1 + t_{d1} = k (l_1 C_o + C_1) + rol_1 Col_1 + C_1 + t\, w1\, 2$

When we simplify the following expression, it is found that the relationship between w_2' and $w_1$is 2.

$w_2' = (l1C0'C1)/ ((l1+l2)Co+C1+C2)w1=(Cleft/Ctotal)w1$

Where the sum of the capacitance downstream in both sub trees is C total and C left is the total capacitance downstream in the sub tree which is on left. Similarly, it can be defined that C right is the total capacitance in the subtree which is on the left, the expression for w′3 can be derived as

$w_3' = (l2C0'C2)/ ((l1+l2) Co+C1+C2)= (Cright/Ctotal)/w1$

Therefore, adding (5) and (6), we obtain the result

$w_1 = w'_2 + w'_3$(7)

The scenario that is shown in Figure 4 (a) is much worse than that in Figure 4(b) when buffer area is considered asw2′ and w3′ are greater than w2 and w3 respectively, and alsow1 = w2' + w3'.Positioning an LHconverter in the tree at lower place is considered to result in cost of smaller area as long we know that the size of LHconverter is always proportional.

Next, Two scenarios are considered in terms of the dissipation of powers how n in Figures 4(a) and 4(b). As before transition time constraints at the sinks are met with each of w_1, w_2 and w^1.

$P=k_1 w+k_2$(8)

The output stage is assumed to be sized in such a way that the ratio of the NMOS transistor to the PMOS are equal.

Therefore, as the scenario of Figure 4 is considered, in order for option (a) to be better than option (b), the

following condition must hold: $k_1 w_1 + k_2 + k_3(L_1 - l) + k_4 (L_2 + l) < k_1 w_2 + k_2 + k_1 w_3 + k_2 + k_3 L_1 + k_4 L_2$ (9)
Where $k_3 = f V_{ddL}^2 C_o$ and $k_4 = f V_{ddH}^2 C_o$.

Theorem 2: The power in the clock tree P1is considered at a specific positioning of the LHconverters, which is sized to meet the transition time constraints at the sinks. Let the power corresponding to LHconverters be P2which is inserted at any location which is high in the tree, appropriately sized to satisfy transition time constraints. The dissipation of power P1< P2but the following condition should hold: $k_2 > k_1(w_1 - (w_2 + w_3)) + l(k_4 - k_3)$ (10)

Proof: Immediately followed from a simplification of (9). It is stated in the inequality in (10) that k_2 must be greater than the sum of the dissipation of power due to the increase in size of the buffers.

In order for (10) to be true, $k_2 > k_1(w_1 - (w_2 + w_3))$ and $k_2 > l(k_4 - k_3)$, as we can see that both terms of the right hand side are positive The expression of the latter condition can be given as $l < k_2/(k_4 - k_3)$

Technology	250	180	150	130	100
V_{ddH}/V_{ddL}	1.38	1.2	1.25	1.25	1.33
Maximum l	26.5	9.7	2.8	7.5	4.9
Benchmarks	r1	r2	r3	r2	r5
Avg*l* to first buffer	463	357	366	315	293

Table1: Required and Average Wire length

2. PROPOSED ALGORITHM

2.1 Outline of the Algorithm

The major difference is in the usage of an HLconverter at the root of the tree and at various points in the clock tree, the use of LHconverters.

Algorithm Bottom-up Buffer Insertion
INPUT: set of sinks S, technology parameters
OUTPUT Tree of buffered merging segments
BEGIN
A = S /* A being a set of non-buffered segments */
B = Φ /* B being a set of buffered segments */ while (|A| > 1 or |B| > 0)
if (|B| > 0) and (|A| = 0)
A = B; B = Φ /*if A is empty and B is non-empty, swap them*/
G (E, V) = DT (A); /* Build Delaunay Triangulation on A */}
I = Find_independent_edges (G);
A = A - {b, c} if (buffer insertion criterion satisfied)

b= insert buffer (b);

c= insert buffer (c);

a= zero merge (b, c); B=B U {a}

Else

A=A U {a}

END

Figure 7: Algorithm Hierarchical Clustering-Based Buffer Insertion

A Delaunay Triangulation on Ais built, and then a nearest neighbor graph is constructed. Form A, the two merged segments will be deleted and the new merging segment will be checked to see whether the transition time constraint is satisfied. Once the first level of clock buffers is added, the sets A and Bare swapped, the whole procedure is repeated again. The algorithm is proceeded until only one node is left and A and B is empty. At this point, a tree of segments is returned by the procedure.

Property: It is ensured by algorithm of Bottom-up Buffer Insertion that there will be an equal number of buffers for any path from the root to the sinks.

2.2 Finding a Minimum Power Solution

For each merging point, a tuple [Sol buffered, Sol unbuffered] is stored. The parameters S buffered and S unbuffered give the best solution for the situation where an LH converter has been added or has not been added to the downstream subtree. At the current level the two S unbuffered solutions are combined to create a S unbuffered solution, whenever two sub trees are merged. A S buffered solution may be created either by combination of the two S buffered solutions from the subtrees, or by combination of the two S unbuffered solutions and an LHconverter is placed at the merging point, which is sized so that the transition time requirements are met at the leaf nodes. This is continued up the tree until the maximum sizeis less than the required buffer size, and this is the point where the optimal solution is chosen.

3. EXPERIMENTAL RESULTS

There are five benchmarks on which our algorithm was tested. The parameters that are used are based on a 250 nm technology and are listed in Table 2. The unit driver resistance is R0; all other parameters are as described earlier.

The comparison of power dissipation between algorithms CLisshown in Table 3 which is augmented with a buffer insertion algorithm and our algorithm. The values of total power as shown in the table are

the sum of the buffer power P_b and the wire power Pw in the clock network. The clock skew is zero by construction according to the delay metrics.

The figures that are shown in Table 3 are based on a 500MHz clock having the transition times which is accounting for 10% of the clock period. Our power minimization algorithm using V_{ddH}=2.5V and V_{ddL}= 1.8V are having the results which are shown next under "Dual V_{dd}." Finally, the results of applying our power minimization algorithm under V_{ddH}=2.5V is shown, with the use of a swing voltage which is lower, V_s that varies from V_{tn} toV_{ddH}-$|V_{tp}|$; it is assumed that V_{tn}= $|V_{tp}|$ = 0.2 V_{dd}. There is a column marked "Low Swing.", these results are presented there. For the benchmarks r1 through r5, 2, 10, 14, 28 and 56 are the number of buffers that are moved one level up from the sinks respectively. For any of these benchmarks ,no buffers are moved more than one level up from the sinks.

Table 2: 250 nm Technology Parameters

Benchmark	CL (mW)	Dual $V_{dd\ (mW)}$	Low Swing (mW)
r1	26.93	13.34(50.5%)	16.31(39.4%)
r2	49.63	27.67(44.2%)	33.43(32.6%)
r3	62.19	35.11(43.5%)	43.80(29.6%)
r4	130.57	71.77(45.0%)	90.44(30.7%)
r5	183.02	105.67(42.3%)	134.62(26.4%)

It can be clearly seen from Table 3 that the power saved whenreduced swing buffers and multiple supply voltages are used are an average of 31% and 45% respectively. An upper bound on the power savings is determined by

ΔP_{max}= 1 - (V_{ddL} 2/V_{ddH} 2) = 52%

4. CONCLUSION

Table 3: Power Dissipation of the Clock Trees

Parameters	Values
C_o	53.1 aF
R_o	0.293 Ω/μm
R_d	17.1 KΩ
C_b	170 aF
f	500 MHz
VddH-VddL	2.5-1.8V

An analysis of the problem of routing of clock tree is presented at different voltages for the purpose of utilization and distribution. It is guaranteed by our implementation that number of buffers is equal along any path from root to sinks, and for the distribution of the clock signal, a low voltage is used before it is converted again to a voltage which is high at the points of utilization. Our algorithm has been applied to the low power clock schemes: Reduced-swing buffers are used in one scheme, while multiple supply

voltages are used by the other.The experimental results show that using our algorithm,the low power clock schemes provide significant savings in the dissipation of total power.

The ideal power reduction is given by [1 –(V_{swing}/V_{dd})] Using a single V_{dd} with a reduced swing and[1-(V_{ddL}2/V_{ddH}2)] using two voltages V_{swing}. Technology constraints such as the maximum electrical field sustainable by the thin oxide will determine the maximum V_{dd} as the device performance is scaled down. The values of minimum V_{ddLOW} and the value of Vs wing both depends on the threshold voltage – scaling in these is not as fast as V_{dd} in future technologies – and considerations on noise, which is going to limit the value of V_{ddLOW}. Therefore, it is expected that the time will be reduced by using two supply voltages using the circuits described in this paper. We believe that significant benefits will be provided by this approach. However, techniques can be invoked using sub threshold logic so that the gains of an approach are maintained that distributes the clock signal at a different value from its value which is at the utilization points.

The procedure which is used for the construction of zero-skew clock trees under is an extended part of techniques that are used nowadays. It is expected that when low voltages are there, techniques of noise avoidance hat are better will be required and buffer insertion techniques are used. Two possibilities are presented by the work in this paper: we can use either two supply voltages that re independent, or a single supply voltage and a level converter that helps in lowering of the distribution voltage of the clock. It depends on the discipline used, that further constraints should be introduced on clock buffers locations of where the same V_{dd} is used in each row, buffer locations cannot be arbitrary. It is expected that the framework presented here can be extended since typical zero-skew algorithms can be extended so that restrictions on buffer locations can be accommodated.

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Image Denoising Using Independent Component Analysis Technique

Vishwajit K. Barbudhe
Assistant Professor, Jagadambha college of Engineering & Technology, Master of Engineering (ME), Electronics & Telecommunication Engineering Department, Yavatmal, India

A B S T R A C T

It is necessary to apply an efficient denoising technique to compensate for such data corruption. Image denoising still remains a challenge for researchers because noise removal introduces artifacts and causes blurring of the images. This paper describes different methodologies for noise reduction (or denoising) giving an insight as to which algorithm should be used to find the most reliable estimate of the original image data given its degraded version. Removing noise from the original signal is still a challenging problem for researchers. There have been several published algorithms and each approach has its assumptions, advantages, and limitations. This paper presents a review of some significant work in the area of image denoising. After a brief introduction, some popular approaches are classified into different groups and an overview of various algorithms and analysis is provided.

Keywords- (Image denoising , Independent component analysis technique)

INTRODUCTION

A quantitative measure of comparison is provided by the signal to noise ratio of the image. A very large portion of digital image processing is devoted to image restoration. This includes research in algorithm development and routine goal oriented image processing. Image restoration is the removal or reduction of degradations that are Incurred while the image is being obtained. Degradation comes from blurring as well as noise due to electronic and photometric sources. Blurring is a form of bandwidth reduction of the image caused by the imperfect image formation process such as relative motion between the camera and the original scene or by an optical system that is out of focus. When aerial photographs are produced for remote sensing purposes, blurs are introduced by atmospheric turbulence, aberrations in the optical system and relative motion between camera and ground. In addition to these blurring effects, the recorded image is corrupted by noises too. A noise is introduced in the transmission medium due to a noisy channel, errors during the measurement process and during quantization of the data for digital storage. Each element in the imaging chain such as lenses, film, digitizer, etc. contribute to the degradation.

Image denoising is often used in the field of photography or publishing where an image was somehow degraded but needs to be improved before it can be printed. For this type of application we need to know

something about the degradation process in order to develop a model for it. When we have a model for the degradation process, the inverse process can be applied to the image to restore it back to the original form. This type of image restoration is often used in space exploration to help eliminate artifacts generated by mechanical jitter in a spacecraft or to compensate for distortion in the optical system of a telescope. Image denoising finds applications in fields such as astronomy where the resolution limitations are severe, in medical imaging where the physical requirements for high quality imaging are needed for analyzing images of unique events, and in forensic science where potentially useful photographic evidence is sometimes of extremely bad quality. Let us now consider the representation of a digital image. A 2-dimensional digital image can be represented as a 2-dimensional array of data s(x,y), where (x,y) represent the pixel location. The pixel value corresponds to the brightness of the image at location (x,y). Some of the most frequently used image types are binary, gray- scale and color images. Binary images are the simplest type of images and can take only two discrete values, black and white. Black is represented with the value „0" while white with „1". Note that a binary image is generally created from a gray-scale image. A binary image finds applications in computer vision areas where the general shape or outline information of the image is needed. They are also referred to as 1 bit/pixel images. Gray-scale images are known as monochrome or one-color images. The images used for experimentation purposes in this thesis are all gray-scale images. They contain no color information. They represent the brightness of the image. This image contains 8 bits/pixel data, which means it can have up to 256 (0-255) different brightness levels. A „0" represents black and „255" denotes white. In between values from 1 to 254 represent the different gray levels. As they contain the intensity information, they are also referred to as intensity images. Color images are considered as three band monochrome images, where each band is of a different color. Each band provides the brightness information of the corresponding spectral band. Typical color images are red, green and blue images and are also referred to as RGB images. This is a 24 bits/pixel image.

LITERATURE SURVEY ON PRINCIPAL COMPONENT ANALYSIS

The two papers adopted different approaches, with the standard algebraic derivation given above being close to that introduced by Hotelling (1933). Pearson (1901), on the other hand, was concerned with finding lines and planes that best fit a set of points in p-dimensional space, and the geometric optimization problems he considered also lead to PCs. In the 32 years between Pearson"s and Hotelling"s papers, very little relevant material seems to have been published, although Rao (1964) indicates that Frisch (1929) adopted a similar approach to that of Pearson.

LITERATURE SURVEY ON ADAPTIVE PRINCIPAL COMPONENT ANALYSIS

One of the main difficulties in using principal component analysis (PCA) is the selection of the number

of principal components (PCs). There exist a plethora of methods to calculate the number of PCs, but most of them use monotonically increasing or decreasing indices. Therefore, the decision to choose the number of principal components is very subjective. In this paper, we present a method based on the variance of the reconstruction error to select the number of PCs. This method demonstrates a minimum over the number of PCs. Conditions are given under which this minimum corresponds to the true number of Pcs.

Ten other methods available in the signal processing and chemometrics literature are overviewed and compared with the proposed method. Three data sets are used to test the different methods for selecting the number of PCs: two of them are real process data and the other one is a batch reactor simulation.

LITERATURE SURVEY ON INDEPENDENT COMPONENT ANALYSIS

The ICA algorithms above only consider the higher order statistics of the separate data maps recorded at different time points, with no regard for the time order in which the maps occur. The so-called „second-order blind identification" (SOBI) approach (Molgedey and Schuster, 1994) considers relationships between multiple time points using an autoregressive model in which sources are assumed to have both differing spatial distributions and stable power spectra. A recent internet search readily found freely available Matlab (The Mathworks, Inc.) platform code for at least 22 methods of ICA decomposition (Makeig and Delorme, 2004).

ALGORITHMS AND DETAILS ON METHODS:- PRINCIPAL COMPONENT ANALYSIS

The central idea of principal component analysis (PCA) is to reduce the dimensionality of a data set consisting of a large number of interrelated variables, while retaining as much as possible of the variation present in the data set. This is achieved by transforming to a new set of variables, the principal components (PCs), which are uncorrelated, and which are ordered so that the first few retain most of the variation present in all of the original variables.

BACKGROUND MATHEMATICS

Statistics

The entire subject of statistics deals with large dataset and its analysis in terms of the relationships between the individual points in that dataset.

Standard Deviation

The Standard Deviation (SD) of a data set is a measure of how spread out the data is. The definition of the SD is: "The average distance from the mean of the data set to a point". The way to calculate it is to

compute the squares of the distance from each data point to the mean of the set, add them all up, divide by (n-1) and take the positive square root. As a formula:

$$s = \sqrt{\frac{\sum_{i=1}^{n} (X_i - X)^2}{(n-1)}}$$

Where s the usual symbol for standard deviation of a sample.

Variance

Variance is another measure of the spread of data in a data set. In fact it is almost identical to the standard deviation. The formula is this:

$$s^2 = \frac{\sum_{i=1}^{n} (X_i - X)^2}{(n-1)}$$

It can be noticed that this is simply the standard deviation squared, in both the symbol (s2) and the formula (there is no square root in the formula for variance). s2 is the usual symbol for variance of a sample. Both these measurements are measures of the spread of the data. Standard deviation is the most common measure, but variance is also used.

Covariance

Standard deviation and variance only operate on 1 dimension, so that it could only calculate the standard deviation for each dimension of the data set independently of the other dimensions. However, it is useful to have a similar measure to find out how much the dimensions vary from the mean with respect to each other.

Covariance is such a measure. Covariance is always measured between 2 dimensions. If you calculate the covariance between one dimension and itself, you get the variance. If there was 3- dimensional data set (x, y, z), then you could measure the covariance between the x and y dimensions, the x and z dimensions, and the y and z dimensions. Measuring the covariance between x and x, or y and y, or z and z would give you the variance of the x, y and z dimensions respectively.

The formula for covariance is very similar to the formula for variance. The formula for variance could also be written like this:

$$var(X) = \frac{\sum_{i=1}^{n} X_i - X \ (X_i - X)}{(n-1)}$$

So given that knowledge, here is the formula for covariance:

$$cov(X, Y) = \frac{\sum_{i=1}^{n} X_i - X \ (Y_i - Y)}{(n-1)}$$

The Covariance Matrix

Covariance is always measured between 2 classes. If we have dataset more than 2 dimensions, there is more than one covariance that can be calculated. A useful way to get all the possible covariance values between all the different dimensions is to calculate them all and put them in a matrix. So, the definition for the covariance matrix for a set of data with n dimensions is:

$C^{n\times n} = C_{i,j}, C_{i,j} = \text{cov}\, Dim_i, Dim_j$

where C^{nXn} is a matrix with n rows and n columns, and Dim_x is the x th dimension.

Matrix Algebra

This section serves to provide a background for the matrix algebra required in PCA.

(I).Eigenvectors: You can multiply two matrices together, provided they are compatible sizes. Eigenvectors are a special case of this. It is the nature of the transformation that the eigenvectors arise from. Imagine a transformation matrix that, when multiplied on the left, reflected vectors in the line y=x.

Then you can see that if there were a vector that lay on the line y=x, its reflection is itself. This vector (and all multiples of it, because it wouldn't matter how long the vector was), would be an eigenvector of that transformation matrix. What properties do these eigenvectors have? You should first know that eigenvectors can only be found for square matrices. And, not every square matrix has eigenvectors. And, given n X n matrix that does have eigenvectors, there are n of them. Given a 3 X 3 matrix, there are 3 eigenvectors.

Another property of eigenvectors is that even if you scale the vector by some amount before you multiply it, you still get the same multiple of it as a result. This is because if you scale a vector by some amount, all you are doing is making it longer, not changing its direction. Lastly, all the eigenvectors of a matrix are perpendicular, i.e. at right angles to each other, no matter how many dimensions you have i.e. orthogonal. This is important because it means that you can express the data in terms of these perpendicular eigenvectors, instead of expressing them in terms of the x and y axes.

Another important thing to know is that when mathematicians find eigenvectors, they like to find the eigenvectors whose length is exactly one. This is because the length of a vector doesn‟t affect whether it‟s an eigenvector or not, whereas the direction does. So, in order to keep eigenvectors standard, whenever we find an eigenvector we usually scale it to make it have a length of 1, so that all eigenvectors have the same length.

(ii). Eigenvalues: Eigenvalues are closely related to eigenvectors. For each eigenvector, the corresponding

eigenvalue is the factor by which the eigenvector changes when multiplied by the matrix.

Calculations of Principal Components

The identification of subspace in which the data approximately lies will be calculated with the help of Principal Components Analysis (PCA) tool.

Suppose we are given dataset $x^{(i)}$; i=1,...,m Lets $x^{(i)} \epsilon K$ for each i (n << m).

To develop the PCA algorithm, we need some preprocessing of data to normalize its mean and variance as follows:

Suppose $\varkappa 1, \varkappa 2, \ldots, \varkappa_M$ are Nx1 vectors

Step 1: Find mean $\bar{x} = \frac{1}{M} \sum_{i=1}^{M} x_i$

Step 2: Subtract the mean: $\Phi_i = x_i - \bar{x}$

Step 3: Form the matrix $A = [\Phi_1, \Phi_2, \ldots, \Phi_M]$ (NxM matrix), then compute:

$$C = \frac{1}{M} \sum_{n=1}^{M} \Phi_n \Phi_n^T = AA^T$$

(Sample Covariance matrix, NxN, characterizes the scatter of the data)

Step 4: Compute the eigenvalues of C: $\lambda_1 > \lambda_2 > \cdots > \lambda_N$

Step 5: Compute the eigenvectors of C: $u_1, u_2, \ldots, u_N$

Since C is symmetric, $u_1, u_2, \ldots, u_N$ form a basis,(i.e. any vector x (or $(x - \bar{x})$ can be written as a linear combination of the eigenvectors): $x - \bar{x} = b_1 u_1 + b_2 u_2 + \cdots + b_N u_N = \sum_{i=1}^{N} b_i u_i$

Step 6: (dimensionality reduction step) Keep only the terms corresponding to the K largest eigenvalues: $x - \bar{x} = \sum_{i=1}^{K} b_i u_i$ where K<<N. The representation of $(x - \bar{x})$ into the basis $u_1, u_2, \ldots, u_N$ is thus

$$\begin{matrix} b_1 \\ b_2 \\ \ldots \\ b_K \end{matrix}$$

How to choose the principal components? To choose K, use the following criterion:

$$\frac{\sum_{i=1}^{K} \lambda_i}{\sum_{i=1}^{N} \lambda_i} > Threshold(e.g., 0.9 \text{ or } 0.95)$$

Geometrical Interpretation

1. PCA projects the data along the directions where the data varies the most.
2. These directions are determined by the eigenvectors of the covariance matrix corresponding to the largest eigenvalues.
3. The magnitude of the eigenvalues corresponds to the variance of the data along the eigenvector directions.

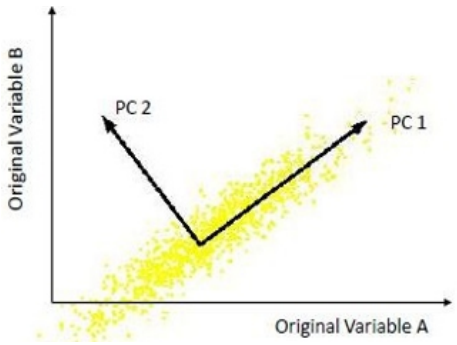

Fig. Principal Components

Properties and assumptions of PCA:-

1. The new variables (i.e., b_i "s) are uncorrelated.
2. The covariance of bi "s is: $U^T C U = \begin{matrix} \lambda_1 & 0 & 0 \\ 0 & \lambda_2 & 0 \\ \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot \\ 0 & 0 & \lambda_K \end{matrix}$

1. The covariance matrix represents only second order statistics among the vector values.

2. Since the new variables are linear combinations of the original variables, it is usually difficult to interpret their meaning.

RESULTS

The Codes are written for PCA, Adaptive PCA, and ICA. These codes are simulated, synthesized and implemented in Matlab. The results of simulation are reported here. The images which are obtained are as follows

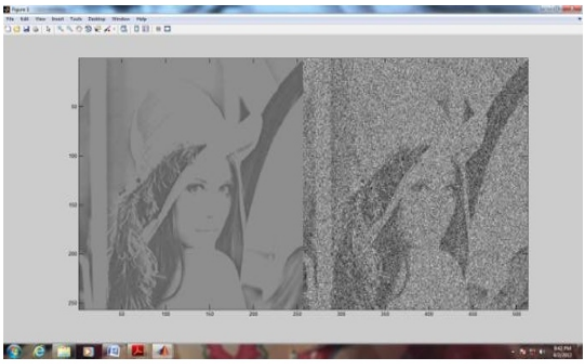

Fig. Original image+ Noisy image

Matlab figure window shows original image in jpg format of 256 X 256 pixels with noisy image having Gaussian noise with signal to noise ratio 6.816146 db, entropy 0.3334 , Variance 234.1728 , Correlation 0.882.

Fig. Noisy image + denoised image(JPG) by PCA

Matlab figure window shows original image in jpg format of 256 X 256 pixels with noisy image having Gaussian noise with signal to noise ratio 7.379763 db, entropy 0.0244, variance 254.7538, correlation 0.0486.

Fig Noisy image + denoised image(JPG) by Adaptive PCA

Matlab figure window shows original image in jpg format of 256 X 256 pixels with noisy image having Gaussian noise with signal to noise ratio 6.936651 db, entropy 0.3216, variance 235.0867, correlation 0.0829.

Matlab figure window shows original image in jpg format of 256 X 256 pixels with noisy image having Gaussian noise with signal to noise ratio 13.704733 db, entropy 0.2117, variance 243.1234, correlation 0.0488.

Matlab figure window shows original image in GIF format of 256 X 256 pixels with noisy image having Gaussian noise with signal to noise ratio 6.962064 db, entropy 0.3217, Variance 235.1129 , Correlation 0.0616 .

Fig Noisy image + denoised image(GIF) by PCA

Matlab figure window shows original image in GIF format of 256 X 256 pixels with noisy image having Gaussian noise with signal to noise ratio 8.099423 db, entropy 0.0237, Variance 254.7873 , Correlation0.0905 .

Fig Noisy image + denoised image(GIF) by Adaptive PCA

Matlab figure window shows original image in GIF format of 256 X 256 pixels with noisy image having Gaussian noise with signal to noise ratio 13.751627 db, entropy 0.0415, Variance 243.1370, Correlation 0.2115

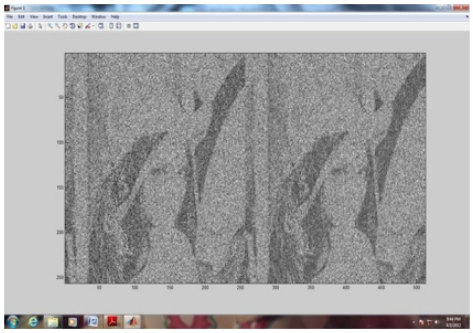

Fig Noisy image + denoised image(GIF) by ICA

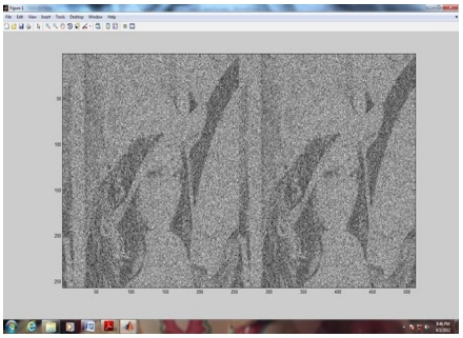

Fig Noisy image + denoised image(BMP) by PCA

Matlab figure window shows original image in BMP format of 256 X 256 pixels with noisy image having Gaussian noise with signal to noise ratio 6.967201 db, entropy 0.3210 , Variance 235.1199, Correlation 0.0616 .

Fig Noisy image + denoised image(BMP) by Adaptive PCA

Matlab figure window shows original image in BMP format of 256 X 256 pixels with noisy image having Gaussian noise with signal to noise ratio 7.809952 db, entropy 0.0238, Variance253.7528 , Correlation0.0906 .

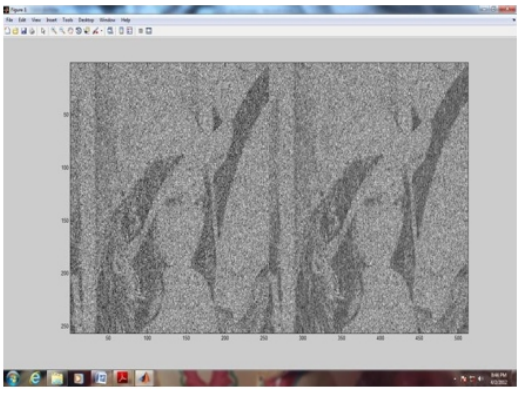

Fig Noisy image + denoised image(BMP) by ICA

Matlab figure window shows original image in BMP format of 256 X 256 pixels with noisy image having Gaussian noise with signal to noise ratio 13.699066 db, entropy 0.2115, Variance 243.1330, Correlation 0.0488.

CONCLUSION

The signal to noise ratio of an image under study is 8.5db. Principal component analysis will achieved an improve value of signal to noise ratio as 8.69db. Adaptive PCA has proven to show an enhanced value of signal to noise ratio upto 11.01db. Adaptive PCA has shown an improvement in noise reduction. Furthermore with independent component analysis with local maxima algorithm we could achieve an further enhancement value upto 15.18db of signal to noise ratio for the image under study. For various type of image format we get the different signal to noise ratio, and by comparing the signal to noise ratio and parameter table we can conclude that ICA is the best tool for the image denoising. The improvement of signal to noise ratio proves that ICA is powerful tool for denoising of an image.

Some preliminary studies have been made about the effectiveness of Independent Component Analysis. So we can conclude that ICA-based methods give, at least for their application, significantly better results than PCA. The superiority of ICA over PCA is also implicit in the use of PCA as a preprocessing step.

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Comparative Study, Design and Simulation of Energy Storage Device For Piezoelectric Energy Harvester

Asharfilal Sharma[1], Ashish Gupta[2]
[1]School of Instrumentation, DAVV, Indore, India.
[2]Chameli Devi Group of Institutions, Indore, India.

ABSTRACT

Piezoelectric materials have been used to transform ambient mechanical vibrations into electrical energy according to the principle of it. The electrical energy thus produced by this principle is too low to directly recharge the rechargeable batteries, so the need is to improve voltage. Therefore in our work we have used the improved voltage as a stored energy to power portable devices. For the above statement we have designed our circuit with the help of modeling, simulation and experimental results for two types of non-adaptive harvesting circuits using TINAPRO software. In our work capacitors have been charged using improved Ottman's et al non-adaptive harvesting circuit to determine the charge time and maximum capacity of a capacitor to which that can be charged, with the help of rectifier and a static converter transform the electrical energy into a suitable form to charge the portable devices. Values of stored electrical power are reported and commented.

Keywords- PZT, PDPE, EHEV, HC

INTRODUCTION

Over the last two decade, several articles have reported the use of transduction mechanisms for low power generation from ambient vibrations. As stated by Williams and Yates[2], there are three basic mechanisms to electric energy conversion that are electromagnetic[3], electrostatic[4] and piezoelectric[5] transductions. The conversion of mechanical vibration-to- electricity was first investigated and proposed by Williams and Yates in 1996 [2].

Piezoelectric materials have been used to transform ambient mechanical vibrations into electrical energy according to the principle of it[1].

The main advantage associated with piezoelectric materials is the flexibility towards energy harvesting. These materials are able to convert mechanical ambient energy into electrical energy because of piezoelectric effect. However, the major limitation faced in the piezoelectric energy harvesting is that the average harvested power is too less. Therefore, usually, some storage means are used to store and accumulate the harvested energy. We are taking references of one of the first researchers to realize the need for power storage circuitry was Starner et al in 1996 that uses the idea of using a capacitor and

rechargeable battery for power harvesting[6]. This concept was taken a step further by Umeda et al in1997, who investigated the use of a capacitor with piezoelectric materials[7]. They theoretically and experimentally tested the circuit in various configurations to determine the optimal design. Shortly after the publication of this work, a power harvesting patent was issued to Kimura et al. in 1998 for a means of storing the energy from a piezoelectric device in a capacitor[8]. Much of the early researches into power harvesting considered the use of capacitors as a way to store energy and have dealt with extracting maximum power from the piezoelectric materials or developing circuitry to store the energy[9]. In our present work firstly we have taken simulated results of two non-adaptive harvesting circuits by designing the appropriate circuit with the help of TINAPRO software. Secondly design a new rectifier element using a schottky barrier diode and taken simulated result of it, by comparing the simulate results of first circuit and second circuit it is concluded that the result of second circuit shows the improved output.

II. PRINCIPLE OF PIEZOELECTRIC EFFECT

The piezoelectric effect was first demonstrated by the Currie brothers in 1880[1]. If the piezoelectric material is subjected to a voltage drop (i.e. an electrical potential difference applied across its electrodes), it deforms mechanically. This is called the converse piezoelectric effect (CPE) and it was deduced mathematically (after the discovery of the direct piezoelectric effect) from the fundamental principles of thermodynamics by Gabriel Lippmann in 1881 and then confirmed experimentally by the Curie brothers.

Following are the two principles of piezoelectric effect:

(a) First form is direct piezoelectric effect (DPE) that describes the material's ability to transform mechanical strain into electrical charge (the material acts as a sensor).

(b) Second form is converse piezoelectric effect (CPE), which is the ability to convert an applied electrical potential into mechanical strain energy (here the material acts as an actuator).

The phenomenon of direct piezoelectric effect (DPE) is shown in Fig.1 [12].

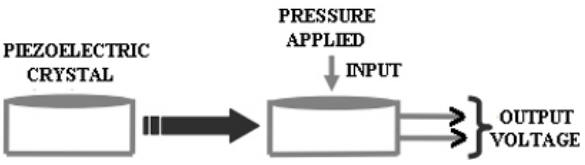

Figure 1: Principle of direct piezoelectric effect (PDPE)

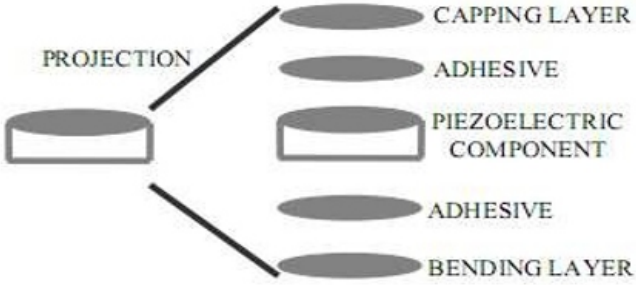

Figure 2: Structure of piezoelectric element

III. Experimental Setup

A. Pulsating DC output of PZT

The electrical energy at the output of the piezoelectric material is a strong and irregular function of time; hence, a full wave bridge rectifier is needed to produce a DC output signal which is shown in Fig. 3. Generally for the rectifier circuit silicon diode is preferred, but the main limitation of these rectifiers is the low power extraction. Therefore we have design bridge rectifier circuit using schottky barrier diode.

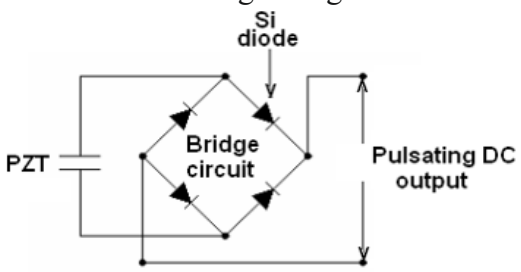

Figure 3: Basic rectifier circuit

The process of experiment was divided into three parts which were energy harvested from vibration environment, harvesting circuit used and improvement made in the Ottoman's Energy harvesting circuit.

B. Energy Harvesting from Vibration Environment (EHEV)

The piezoelectric material selected for a power harvesting application can have a major influence on its functionality and performance. Most common type of piezoelectric material used in power harvesting applications is lead zirconate titanate, piezoelectric ceramic, or piezo ceramic also known as PZT. The piezoelectric device used in this experiment consists of a brass plate with a piezoelectric patch (PZT) bonded on its surface. The dimension of piezoelectric device used is shown in Fig. 4. The thickness of brass plate and piezoelectric patch were 0.4 mm and 0.2mm respectively. The PZT used is flexible as it allows high deflection and it could sensation high pressure.

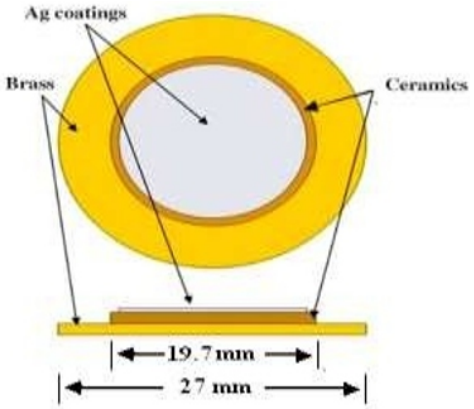

Figure 4: Dimensions of piezoelectric element

When the piezoelectric material is subjected to the pressure produces equivalent electrical signal as a direct piezoelectric effect (DPE). As the frequency of mechanical vibration with pressure applied increases, the output power from piezoelectric material also increases. Based on piezoelectric fundamentals, the behavior of piezoelectric device is investigated for the resonant frequency. The value

of resonant frequency is taken as 50 Hz and maximum generated voltage is 10 volts. The experimental setup for this experiment is shown in Fig. 5.

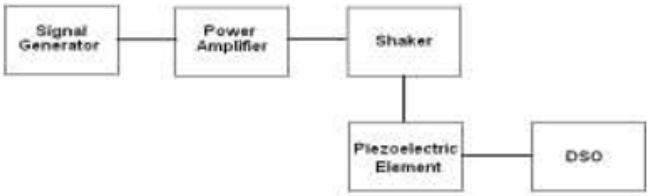

Figure 5: Block diagram of Experimental setup

C. Harvesting Circuit used (HC)

There are two types of non-adaptive harvesting circuits considered by Guan et al., [11] and Ottman et al., [10]. Fig. 6.1(a, b) show the type of circuits considered.

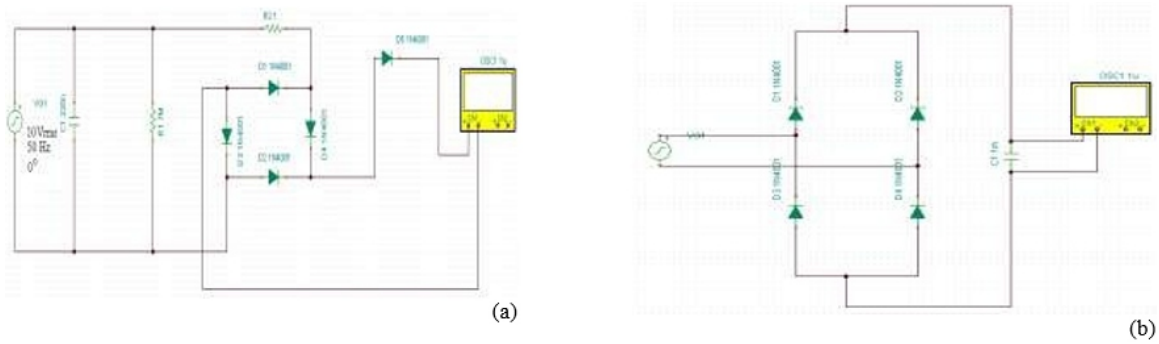

Figure 6.1: Harvesting circuits (a) proposed by Guan et al[11] and (b) by Ottman et al[10]

Both the circuits shown in Fig.6.1 (a ,b) is analyzed using TINAPRO software which uses sinusoidal input frequency of 50 Hz & maximum voltage of 10 V given as source. The output from both the circuit is shown in Fig. 6.2.

Figure 6.2: Output voltage obtained using circuit used by Guan's circuit (a) and used by Ottman's circuit (b)

From the Fig. 6.2 (a), we see that output voltage using Guan's circuit have more ripples where as the output voltage from Ottoman's circuit was in steady state nearing to peak value 9 V . This is due to the use of capacitor in the circuit Fig. 6.1 (b).In the present study the Ottoman's non-adaptive harvesting circuit has been used throughout this study.

D. Improvement made in ottoman's energy harvesting circuit

As the maximum output voltage from piezoelectric material is 10 V we have replaced Silicon diodes used by Ottoman's by Schottky barrier diode because this diode has voltage drop about 0.33 V where in Silicon diode, this value would drop approximately 0.66 V. Energy storage devices used are capacitors of capacities of 0.1F, 0.22F, 1.0F and 1.5F with voltage rating of 10.5V. The experimental setup is shown in Fig. 7.

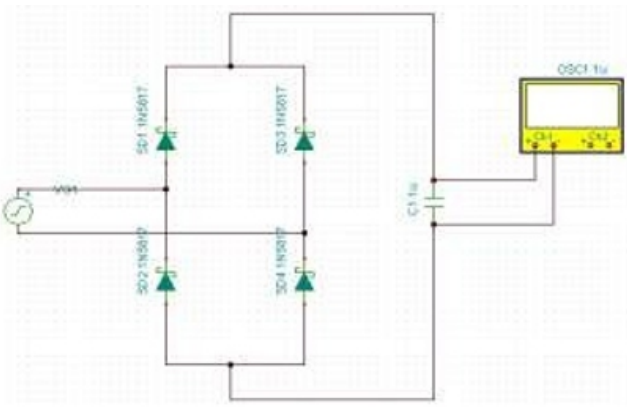

Figure 7: Full wave rectifier using Schottky barrier diodes

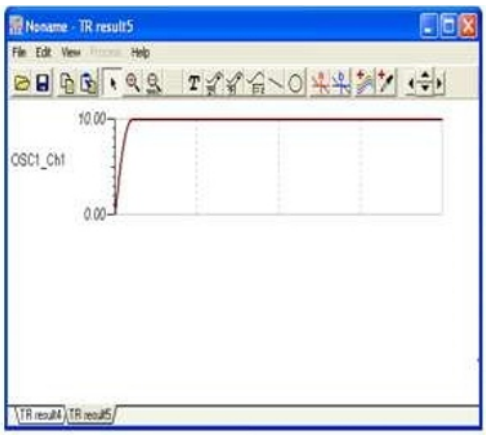

Figure 8: Output voltage by using Schottky barrier diodes

From the simulation results from TINA PRO software it is summarized that the Schottky barrier diode is the best element for rectification as shown in Fig.8.

IV. TESTS CONDUCTED ON VARIOUS STORAGE DEVICES

There are four storage devices tested in order to see the performance of storing energy generated from piezoelectric element and rectifier circuit. Experiments are performed using 50Hz frequency signal. The results are shown in Fig. 9.1 and 9.2.

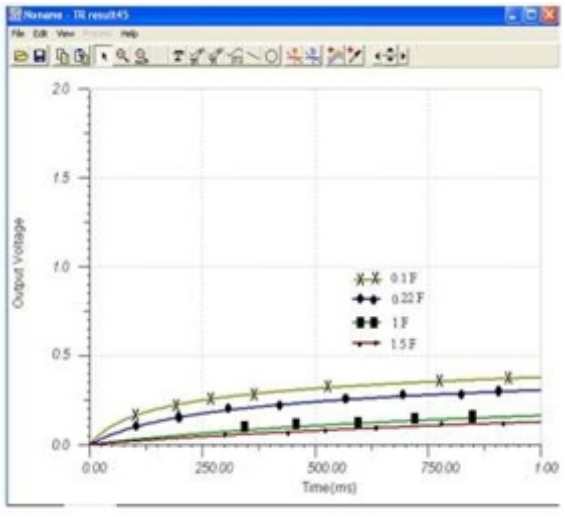

Figure 9.1: Output voltage using Silicon diodes

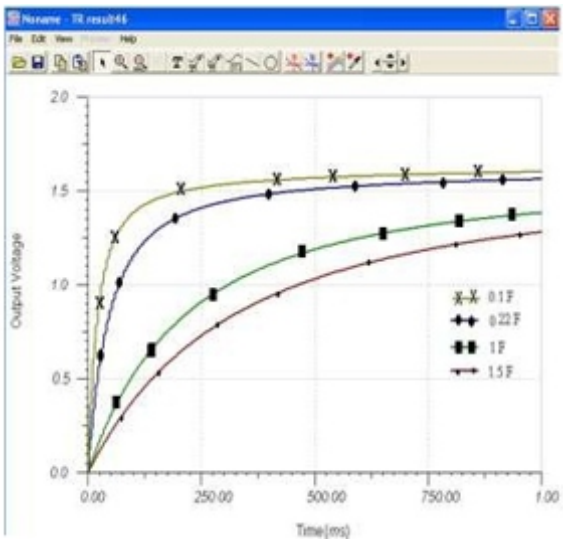

Figure 9.2: Output voltage using Schottky barrier diodes

V. RESULT

From the above simulations it is observed that the capacitor having the value of 0.1F can be charged to maximum output voltage of 1.5 volts using Schottky barrier diode with in 125 ms and same capacitor having the value of 0.1F can be charged to maximum output voltage of 250 mV by using Silicon diode with in 750 ms

VI. FUTURE SCOPE

The proposed work portrays the concept of piezoelectric energy harvesting and from the results it is obvious that if the dimension of piezoelectric material is large than more electrical energy can be obtained which can be used to charge the capacitor to greater extent for the further application. Therefore based on dimension and operating frequency of piezoelectric material various applications requirement will be meet.

VII. CONCLUSION

The main objective of this research is to study and analyze the potential of piezoelectric sensor and element of rectifier circuit as a mean of harvesting energy. To achieve the objective, experimental study had been done where piezoelectric device been used to charge capacitor from vibration environment. It has been proved that electrical power can be generated through piezoelectric material from pressure applied. The study proved that the converted energy can be stored as proven through charging a battery.

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AUTHORS INFORMATION

Prof. A.L. Sharma has teaching and research experience of about 43 years. He worked in several universities in India and abroad. He has published more than 60 research papers in the journals of International repute and has successfully guided six scholars for their PhD degree. His area of specialization is electronics and Instrumentation and materials science.

Ashish Gupta has teaching experience of about 17 years. He has completed his Bachelor of Engineering in 1997 and Master of engineering in 2006 with specialization in Digital Instrumentation. Presently he is pursuing his PhD in guidance of Prof. A.L. Sharma.

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