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Journal of Electrical Engineering and Advanced Technology

Aims and Scope

Journal of Electrical Engineering and Advanced Technology is a journal that publishes original research papers in the fields of Electrical Engineering and Advanced Technology and in related disciplines. Areas included (but not limited to) are electronics and communications engineering, electric energy, automation, control and instrumentation, computer and information technology, and the electrical engineering aspects of building services and aerospace engineering, Journal publishes research articles and reviews within the whole field of electrical and electronic engineering, new teaching methods, curriculum design, assessment, validation and the impact of new technologies and it will continue to provide information on the latest trends and developments in this ever-expanding subject.

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Contents

Reactive Power Compensation Using 500kv, 180 km Line to Maintain Substantially Flat Voltage Profile At All Levels of Ac Transmission System

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ABSTRACT

The global economic recession has contributed in o small measure, in the increasing number of blackouts throughout the world as a result of voltage instability and collapse. The environmental consideration has also contributed by arresting the commission of new power stations and transmission lines, thus resulting in overload of the existing system. This calls for a change to a new direction by using the power system tool-box in MATLAB to stem down the tide. The results showed a balanced system, as confirmed by a substantial flat voltage profiles at all levels during transmission.

Keywords: Reactive Power, Compensation, Power System Tool-Box, Transmission Line, Voltage Collapse, Instability, Balanced System.

1. INTRODUCTION

The function of power system is to provide every consumer, an electricity supply within tight bounds of frequency and voltage level while allowing them to switch appliances at will any time. The consumers also expect a reliable and secure supply of electricity even though they (consumers) are widely scattered and linked by extensive network of lines, cables and transformers which supply the electricity from distant power stations [1]. To meet these tasks, the power utility companies are faced with difficult technical problems coupled and complicated by financial constraints. Going memory lane, the turning points of these problems have been the 1973 – 4 oil crisis which besides leading to a dramatic increase of fuel prices had set off a world-wide economic recession that severely curtailed the growth of electricity demand [8]. The financial repercussions have severely constrained the electricutilities in their outlays on the power networks, at the very time when fuel costs radically altered generation patterns, leading to much higher loading on the interconnections within the transmission grid. Since this global economic recession, difficulties have emerged and worsened as environmental considerations have delayed or resisted the commissioning of new power stations and transmission lines [8].

All these factors have contributed to the changing modes of power system operation, where each utility had been self-sufficient before but are now interdependent on neighbors because of heavy power interchanges. Although, there have been advances in the operational control of power system [4], these have not kept pace with the growing operational complexities. The results of these difficulties have been the increasing number of blackouts throughout the world, many due to system voltage instability. This calls for the need for a new direction in power system control to overcome the present technical difficulties as well as gaining economies for the power utilities. Reactive power compensation by employing the power system tool-box offers an opportunity to develop a new direction for power system control.

2. REACTIVE POWER COMPENSATION

Reactive power compensation can be defined as the management of reactive power to improve the ac power system performance. It is the supply of reactive power in a transmission system to increase the transmittable power, thereby making it compatible with the prevailing load demand. Therefore dynamic compensation is the reactive power compensation that is able to adjust its reactive power automatically so that the concerned system power factors are maintained within the desirable limits. The concepts of Volt Ampere Reactive (VAR) compensation embraces a wide and diverse field of both system and consumer problems, especially related with power quality issues since most of the power quality problems can be attenuated or solved with adequate control of reactive power [3]. The above topic tries to analyze the need for reactive power balance and voltage control in ac transmission lines with a view of contributing its own quota in solving one of the major problems and challenges in power system engineering. In general, the problem of reactive power compensation can be viewed from two perspectives (i) Load compensation and (ii) Voltage support. In load compensation, the objective is to increase the value of the systempower factor to balance the real power drawn from the a.c. supply, compensate voltage regulation and eliminate current harmonic components produced by large and fluctuating nonlinear industrial loads [6]. Voltage support is generally required to reduce voltage fluctuation at a given terminal of a transmission line in order to balance the system.

Reactive power compensation in a transmission line improves the stability of a.c. system by increasing the maximum active power that can be transmitted. It also helps to maintain a substantially flat voltage profile at all levels of power transmission, increases transmission efficiency, controls steady-state and temporary over voltage [3], and can avoid disastrous blackouts [2].

3. VOLTAGE COLLAPSE OR VOLTAGE INSTABILITY

Voltage collapse or instability is the process by which instability leads to loss of voltage in the significant part of the system. Here voltage may be lost due to "angle stability as well. Voltage instability is of increasing importance to utility companies and instability and collapse incidents have been reported in the literature [6], for instance:-

I. In the US pacific northwest, transient stability including transient damping) have usually limited power transfer capability.

II. Also in recent years, the BC hydro has experienced limitations in power transfer capability in its service area of Vancouver, BC, during heavy winter load.

III. Again coming home, voltage stability is also a major concern in Lagos or Abuja area, the rapidly growing metropolitan communities in Nigeria, where peak power demands are increasing.

Also from the available literature and background studies, voltage instability or collapse or sag are characterized by the progressive fall of voltage which can take several forms [6].

- The inability of the network to meet a demand of the reactive power.
- Instability may be triggered by some form of disturbance, resulting in changes of the reactive power requirements.
- Disturbance may result from either small or large changes of essential load.

Detection and Prevention of Voltage Collapse or SAG

The process by which instability leads to loss of voltage in the significant parts of the system is the voltage collapse. While voltages may be lost due to "angle stability" as well, the phenomenon in many instances may be due to a deficit in reactive power generation, loss of critical lines, or degradation of control on key buses [5]. This calls for a new direction in power system to maintain substantially flat voltage profiles at all levels of ac transmission system, using the power system tool-box organized by Hadi sadat. The results indicated a balanced system. However, other preventive measures include, the use of optimal power flow strategy etc to minimize the voltage deviation.

4 LINE PERFORMANCE FOR 500KV, 180KM TRANSMISSION LINE ON NO- LOAD CONDITION, USING POWER SYSTEM TOOL-BOX

The power system tool box is that containing a set of M-files and was developed by Hadi Sadat to assist in typical power system analysis. Some of the programs, such as power flow, optimization, short-circuit and stability analysis were originated and developed by him for a main frame computer while working with power system consulting firms many years ago. These programs have been refined and standardized for interactive use with MATLAB for many problems related to the operations and analysis of power systems. The software modules are structured in such a way that the user may mix them for other power system analyses.

The M-files for typical power system analysis are designed to work in synergy and communicate with each other through the use of some global variables.

Line Performance Program

A program called **LinePerf** is developed for the complete analysis and compensation of a transmission line. The command **LinePerf** displays a menu with five options for the compensation of the parameters of the p models and transmission constants.

(I) Computer Analysis and Details for, 500kv, 180km Line Using Power System Tool- Box in Matlab for No-Load (Open-Circuited) with Shunt Reactor Compensation

3Φ line, 180KM long; Vs = 500KV (L – L); f = 50Hz.

Line parameters are as follows:

r = 0.016W/Km, L = 0.97mH/Km, C = 0.0115mF/Km.

Assume a lossless line.

The command:

>> LinPerf, displays the following menu

Transmission Line Model

Type of parameters for input	***Select***
Parameters per unit length	
r(ohms), g(siemens) L(mH) & C (micro F)	1
Complex z and y per unit length	
r+j*x (ohms/length), g+j*b (siemens/length)	2
Nominal pi or Eq. pi model	3
A, B, C, D constants	4
Conductor configuration and dimension	5
To quit	0

Select number of menu --> 1

Enter Line length = 30

Enter Frequency in Hz = 50

Enter line resistance/phase in ohms per unit length r = 0.016

Enter line inductance/phase in millinery per unit length L= 0.97

Enter line capacitance/phase in micro F per unit length C=0.0115

Enter line conductance/phase in siemens per unit length g= 0

Enter 1 for Medium line or 2 for long line --> 1

Nominal pi model

Z = 0.48 + j 9.14203 ohms

Y = 0 + j 0.000108385 Siemens

$$ABCD = \begin{matrix} 0.9995 \quad + j\ 2.6012e\text{-}005 & 0.48 \quad + j\ 9.142 \\ -1.4097e\text{-}009 + j\ 0.00010836 & 0.9995 + j\ 2.6012e\text{-}005 \end{matrix}$$

Hit return to continue

At this point the program list menu is automatically loaded and displays the following menu

Transmission Line Performance

Analysis	***Select***
To calculate sending end quantities for specified receiving end MW, Mvar	1
To calculate receiving end quantities for specified sending end MW, Mvar	2
To calculate sending end quantities when load impedance is specified	3
Open-end line & inductive compensation	4
Short-circuited line	5
Capacitive compensation	6
Receiving end circle diagram	7
Laudability curve and voltage profile	8
To quit	0

Select number of menu --> 4

Enter sending end line-line voltage kV = 500

Enter receiving end voltage phase angleø (for Ref. enter 0) = 0

Open line and shunt reactor compensation

Vs = 500 kV (L-L) at 0ø

Vr = 500.248 kV (L-L) at -2.60253e-005ø

Is = 31.2958 A at 89.9993ø PFs = 1.30159e-005 leading

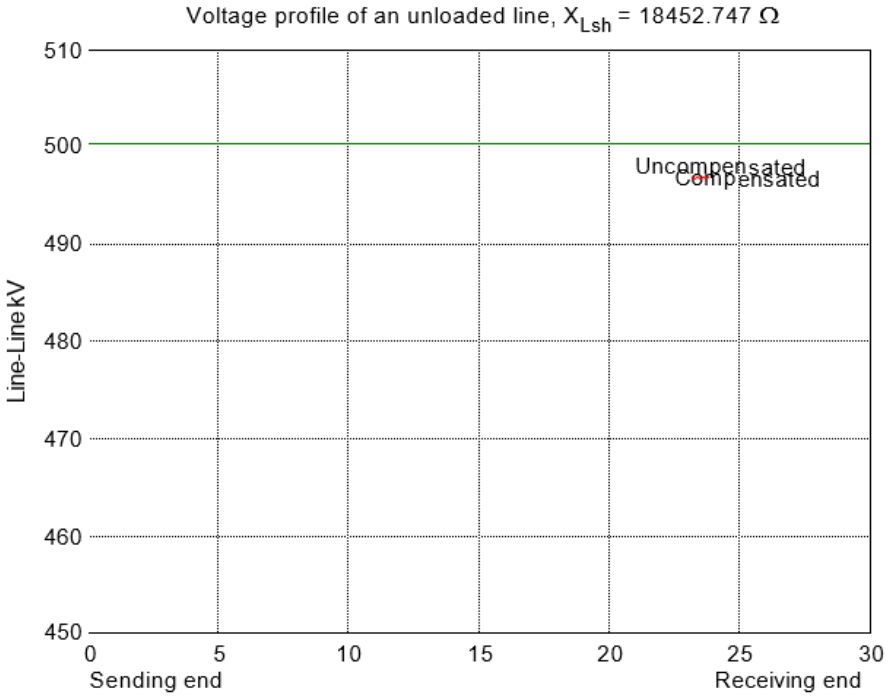
Desired no load receiving end voltage with shunt reactor compensation kV (L-L) = 500

Desired no load receiving end voltage = 500 kV

Shunt reactor reactance = 18452.7 ohm

Shunt reactor rating = 13.5481 Mvar

Hit return to continue



Similar other values and voltage profiles were obtained for: **60km**

Open line and shunt reactor compensation

Vs = 500 kV (L-L) at 0ø

Vr = 500.993 kV (L-L) at -0.000104256ø

Is = 62.6382 A at 89.997ø PFs = 5.21798e-005 capacitive leading

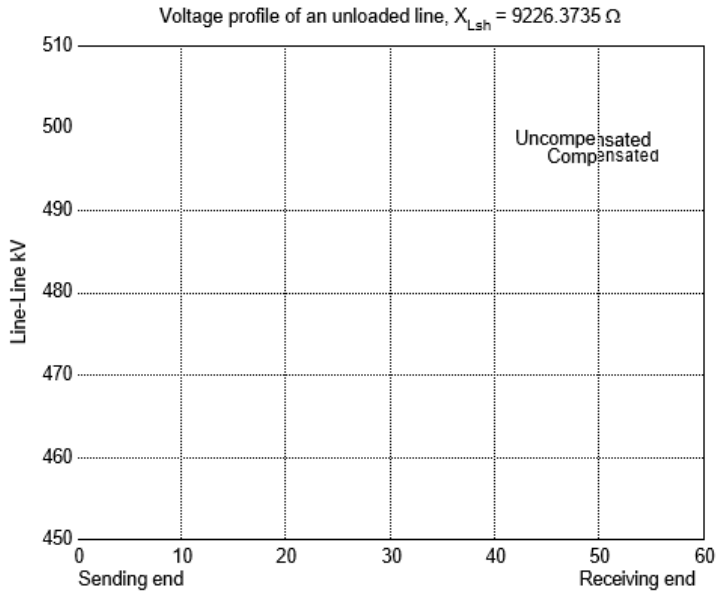
Desired no load receiving end voltage with shunt reactor compensation kV (L-L) = 500

Desired no load receiving end voltage = 500 kV

Shunt reactor reactance = 9226.37 ohm

Shunt reactor rating = 27.0962 Mvar

Hit return to continue



90km

Open line and shunt reactor compensation

Vs = 500 kV (L-L) at 0ø

Vr = 502.239 kV (L-L) at -0.00023516ø

Is = 94.0743 A at 89.9932ø PFs = 0.000117843 leading

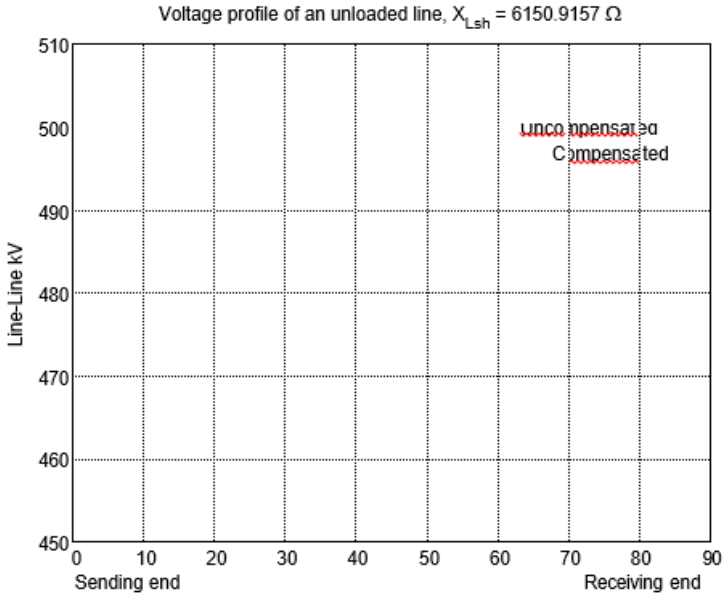
Desired no load receiving end voltage with shunt reactor compensation kV (L-L) = 500

Desired no load receiving end voltage = 500 kV

Shunt reactor reactance = 6150.92 ohm

Shunt reactor rating = 40.6444 Mvar Hit

return to continue



120km

Open line and shunt reactor compensation

Vs = 500 kV (L-L) at 0ø

Vr = 503.995 kV (L-L) at -0.000419524ø

Is = 125.652 A at 89.9879ø PFs = 0.000210597 leading

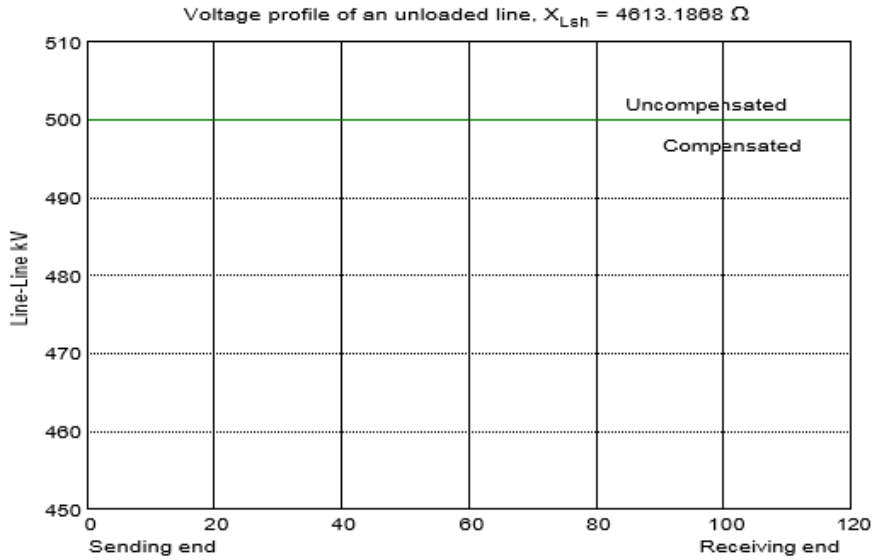
Desired no load receiving end voltage with shunt reactor compensation kV (L-L) = 500

Desired no load receiving end voltage = 500 kV

Shunt reactor reactance = 4613.19 ohm

Shunt reactor rating = 54.1925 Mvar

Hit return to continue



150km

Open line and shunt reactor compensation

Vs = 500 kV (L-L) at 0ø

Vr = 506.27 kV (L-L) at -0.000658465ø

Is = 157.421 A at 89.981ø PFs = 0.000331284 leading

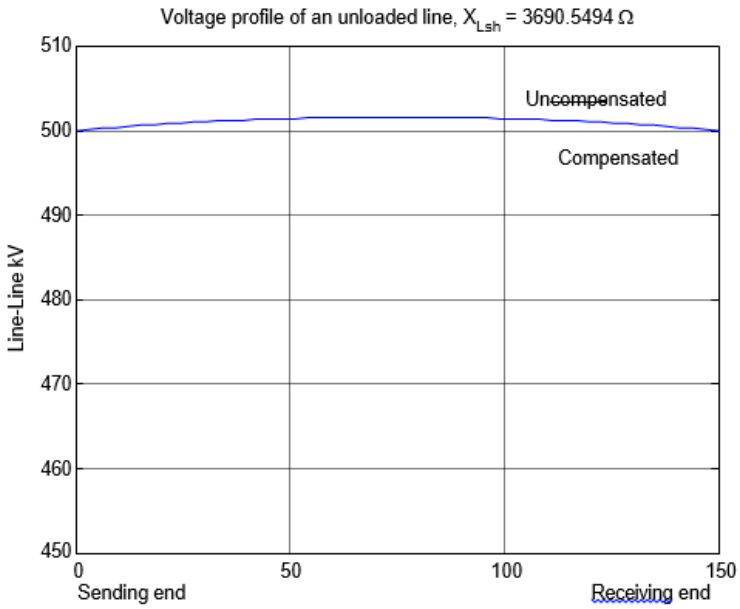
Desired no load receiving end voltage with shunt reactor compensation kV (L-L) = 500

Desired no load receiving end voltage = 500 kV

Shunt reactor reactance = 3690.55 ohm

Shunt reactor rating = 67.7406 Mvar Hit

return to continue



180km

Open line and shunt reactor compensation

Vs = 500 kV (L-L) at 0ø

Vr = 509.079 kV (L-L) at -0.000953451ø

Is = 189.433 A at 89.9724ø PFs = 0.000481015 leading

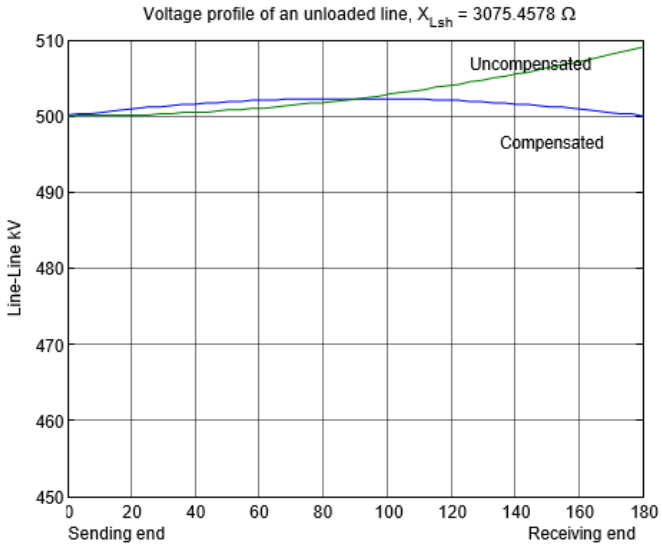
Desired no load receiving end voltage with shunt reactor compensation kV (L-L) = 500

Desired no load receiving end voltage = 500 kV

Shunt reactor reactance = 3075.46 ohm

Shunt reactor rating = 81.2887 Mvar

Hit return to continue



(II) Results

Table 4.1: Showing the results of shunt reactor compensation details for 500KV, unloaded 180KM line (open circuited).

Line Performance for Specified Receiving end Quantities

BEFORE COMPENSATION			AFTER COMPENSATION					
TRANS= MISSION DISTANCE		TR. LINE PARAMETERS				DESIRED N0 LOAD	SHUNT REACTOR	SHUNT
LENGTH OF LINE	CUMU-LATIVE LENGTH OF LINE	PER PHASE r = 0.016Ω/KM L=0.97`MH/KM C=0.0115µl/KM				RECEV. END VOLTAGE	REACTANCE X_{LSH}	REACTOR RATING
(K_M)	(K_M)	V_S (KV)	I_S(A)	V_R(K_V)	I_R(A)	(K_V)	(Ω)	(M_{VAR})
0	30	500	21.31∠90^0	500.248	0	500	18446.83	13.550
30								
	60	500	62.66∠90^0	500.992	0	500	9223.69	27.104
60								
	90	500	91.15∠90^0	502.238	0	500	6146.02	40.677
90								
	120	500	125.83∠90^0	503.990	0	500	4606.63	54.270
120								
	150	500	157.75∠90^0	506.528	0	500	3682.87	67.882
150								
	180	500	190.00∠90^0	509.050	0	500	3066.72	81.520
180								

(III) Observations

The voltage profiles of the compensated lines are substantially flat, almost at all levels of the transmission line, although beyond 120km or more, experienced little divergence. This canbe eliminated by ensuring that the var demand of the load must be met locally by employing positive var generator (Condenser).

Again from table 4.1, Mvar demand (reactive power) increase as the line length increases, and if the var demand is large, the voltage profile at that point tends to sag rather sharply while the compensated and uncompensated profiles diverge more and more as the line length increases.

Moreover, with the constant sending-end voltage (Vs) at 500KV (see the table), the receiving-end voltage will continue to rise with increase in the line length until a quarter of wavelength (l/4) or 1200Km is attained, when the rise becomes infinitely high. And beyond this value to about 1500Km, it may even turn to negative. This rise in voltage at the receiving end is due to the flow of line charging capacitive current through the line inductance. This phenomenon is called Ferranti effect.

CONCLUSION

From the analysis results, reactive power compensation not only maintain substantially flat voltage profiles at all levels of a.c. transmission system as can be seen from the figures in 30km – 180KM lines, the result is that it increases the transmission line efficiency, maintains steady state and temporary over-voltage, and can avoid disastrous blackouts.

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Three Phase Self Excited Induction Generator Electronic Load Controller Using Pi Controller

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A B S T R A C T

A mathematical model of the Self-Excited Induction Generator is developed in this paper. The single point operation of these generators is realized. The voltage of generators remains constant under various operating loads conditions. The Electronic Load Controller is also modelled. The proposed electrical system are modelled and simulated in MATLAB using Simulink and Sim Power System set toolboxes. On the basis this model different characteristics of SEIG with ELC are analyzed.

Keywords: Self excited induction generation, electronic load controller, voltage stability, frequency stability.

INTRODUCTION

The demand for green energy sources has led to the development in the field of solar power and wind power but as both is dependent on external factors such as weather conditions; problems remain with assuring a stable energy supply. Wind power generated using a self-excited induction generator has a drawback in that generated voltage varies with wind velocity. Induction generators are widely used in generating energy from renewable energy resources because they have rugged construction. These generators are simple, reliable, and cost effective, require little maintenance; has self-protection feature against overload, and does not require a DC exciter. However, a great disadvantage of self- excited induction generators is poor voltage regulation and its value depends on the prime mover speed, capacitance, load current and power factor of the load. Another disadvantage is complex calculations for excitation capacitance. A stand-alone induction generator requires a capacitor bank to be connected across the generator terminals, which is the only source of magnetizing current. Also for build-up of voltage to occur, remnant magnetism must be present in the rotor. Therefore, we need a control system is to regulate the voltage to meet the constant voltage demand.

SELF-EXCITED INDUCTION GENERATOR

SEIG has cage rotor construction with shunt capacitors connected at its terminals for excitation; which may be either constant or variable. It is also called as an asynchronous generator because the speed during induction generator operation is not synchronous. With sufficient capacitors connected across each of induction motor terminals; 3 phase induction motor works as a Self-Excited Induction Generator. Self-excitation of the generator begins by the action of either a residual magnetism of the iron core or charge in the excitation capacitors. When the induction machine is driven by a prime mover, the residual magnetism of the iron core induces voltages in the stator windings at a frequency proportional to the rotor speed. With sufficient capacitor excitation and minimum load impedance, the process continues leading to increase in induced stator voltage. It settles to a steady state operating point determined by the air gap flux linkage-saturation. The machine now operates as a Self- excited Induction Generator.

ELECTRONIC LOAD CONTROL OF SELF-EXCITED INDUCTION GENERATORS

An electronic voltage regulator consists of a chopper switch (IGBT), a universal bridge, rectifier, a filtering capacitor and a PI controller. A dump load, controlled by an electronic load controller, is connected across the generator in parallel with the consumer load to keep the net power output across the generator constant. The amount of power required to be dumped in the dump load is decided by the controller. The uncontrolled rectifier is used to converts the SEIG ac terminal voltage into dc. This dc output has the ripples, which must be filtered out and, therefore, a filtering capacitor is used which smoothen the dc output voltage. A suitable gate driver circuit has been developed that turns on the chopper switch when the consumer load on SEIG is less than the rated load and turns off the chopper switch when consumer load on the SEIG is at a rated value. When the IGBT is switched on, the current flows through the dump load and consumes the difference power. It results in a constant load on the SEIG and, hence, constant voltage and frequency at the load terminal. ELC has a drawback that the voltage rating of uncontrolled rectifier and chopper must be same. Another limitation of ELC is that it is introduce a lot of harmonics in the system.

SIMULATION RESULT

The power is almost constant at 7.5 KW. The speed of the generator is 1440 rpm and its terminal voltage is 400 Volts. Its RMS Voltage is 415 Volts.

CONCLUSION

The working of a three phase self-excited induction generator electronic load controller using IGBT choppers and PI controller has been studied. The simulation of scheme has been successfully completed. The output voltage has been obtained as constant thus ensuring satisfactory operation. The power is almost constant at 7.5 KW. The variation in the consumer load is neutralized by diverting the extra power to a dump load. This permits the use of turbine with no flow regulating and their governor control system. Thus SEIG generates constant voltage and constant frequency; as the electrical load is maintained constant at its terminals.

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Design and Analysis of Low Power High Speed Body Bias Controlled Current Latch Sense Amplifier

Pradeep Kumar Kumwat[1‡], Gajendra Sujediya[2]
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[2]Astt. Professor, RIET, Jaipur

ABSTRACT

Sense amplifiers are extensively used in memory. Sense amplifiers are one of the most vital circuits in the periphery of CMOS memories. We know that memory is the heart of all digital systems. Today all worlds are demanding high speed and low power dissipation as well as small area. We know that speed and power dissipation of memory is overall depends upon the sense amplifier we used and their performance strongly affects both memory access time, and overall memory power dissipation. So it is important to design a good sense amplifier which performs well in both speed and power dissipation. In this dissertation, an implementation of a most efficient sense amplifier is done by comparing the best known sense amplifier in today. The dissertation focuses on design, simulation and performance analysis of sense amplifiers.

In this paper, current latch sense amplifier and body bias controlled current latch sense amplifier are designed and results compared. The result shows that the body bias controlled current latch sense amplifier is performing best. The result also shows a novel sense amplifier which consumes small power at same time its speed is faster than other sense amplifiers.

All the designs have been implemented, synthesis and simulated on 180nm CMOS technology using tanner tool version 13.1.

INTRODUCTION

Digital system design in an amazing and emerging field now days. Each and every digital system has adequate memories. In memory today the CMOS memories are used in a much greater quantity than all the other types of semiconductor integrated circuit. SRAMs are used as large caches in microprocessor cores and serve as storage in various inputs on a system-on-chip like graphics, audio, video and image processors. SRAMs also used in high performance microprocessors and graphics chips so for each generation to bridge the increasing divergence in the speeds of the processor and the main memory we need high speed requirements. At the same time, SRAMs used in application processors which go into mobile, handheld and consumer devices have very low power requirements. So power dissipation has become an important consideration both due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated appliances. As with other integrated circuits today, CMOS memories are required to increase speed, improve capacity and maintain low power dissipation.

To read the contents of this memory a sense amplifier is used. The sense amplifier converts the arbitrary logic levels of bitlines to the digital logic levels which required running the peripheral Boolean circuits of outside world of memory. In the SRAM data path, switching of the bitlines, I/O lines and biasing the sense amplifiers consume a significant fraction of the total power. Mainly performance of memory depends on the performance of SA such as delay and power dissipation.

So the sense amplifier is one of the most circuits in the periphery of CMOS memories. Speed and power dissipation of the memory is mainly depends on types of sense amplifier used. So performance of SA strongly affects both memory access time, and overall memory power dissipation.

Power dissipation was not the main issue' just proper output and the circuit operation was the main preference. The low power intend in circuit design is used because of:

1. If the system dissipates high power, then extra design is required for the cooling system, thus the system will become very bulky and will not be portable
2. Due to the extra cooling system the cost of the system will increase.
3. Due to the sky-scraping power dissipation the performance and reliability of the system decreases
4. Memory is the main and important field of design. Today the size of the memory is decreasing and the storing capacity is increasing. As the storing capability is increasing, the time response for the data writing and reading from the memory should be very fast. For this purpose different types of sense amplifiers are used.

NECESSITY OF SENSE AMPLIFIER

In the memory, it is common to reduce the voltage swing on the bit lines to a value significantly below the supply voltage. This reduces both the propagation delay and the power consumption. Noise and other disturbances may be occurred in the memory array for this sufficient noise margin is obtained even for these small signal swings. During the interfacing of the memory to the external field, the amplification of the internal swing is required. This is achieved by the sense amplifiers. Design of a high performance and efficient sense amplifier is very important for design SRAMS but with increasing parameter variations, the developing of a reliable and fast sense amplifier is a big problem in itself Sense amplifiers play a major role in the functionality, performance and reliability of memory circuit. Reduction in delay and power is acquired by using sense amplifier in memory circuits.

The designed sense amplifier should be standard and capable to support the current SRAM design without significantly affecting the other devices of peripherals of SRAM.

BASIC OF SENSE AMPLIFIER

A sense amplifier is an active analog circuit that reduces the time of signal propagation from an accessed memory cell to the logic circuit located at the periphery of the memory cell array, and used to detect small variation on bitlines of memory and produce full voltage swing it means that converts the arbitrary logic levels occurring on a bitline to the digital logic levels of the peripheral Boolean circuits. The sense amplifier circuit has to operate within the conditions which are set by the operation margins. Operation margins in a digital circuit are those domains of voltages, current and charges. These domains unambiguously represent data throughout the entire operation range of the circuit. Operation margin depends on the circuit design, processing technology and environmental conditions. Sense amplifiers, used with memory cells, are key elements in defining the performance and environmental tolerance of CMOS memories. Because of their great importance in memorydesigns, sense amplifiers became a very large circuit-class. CMOS memories are used in a much greater quantity than all the other types of semiconductor integrated circuits, and appear in an amazing variety of circuit organizations.

Memory Sensing and amplifying the information signal which transfers over memory cell to bit lines are the most important ability for a sense amplifier. However, to sense the data correct and fast turn into more and more difficult when the operational voltage scales down to low voltage. In an integrated circuit "sensing" means the recognition and resolve of the data content of a selected memory cell. The sensing may be "nondestructive," when the information content of the selected memory cell is unaffected (e.g., in SRAMs, ROMs, PROMS, etc.), and "destructive," when the information content of the selected memory cell may be altered (e.g., in DRAMS, etc.) by the sense operation. Sensing is performed in a sense circuit.

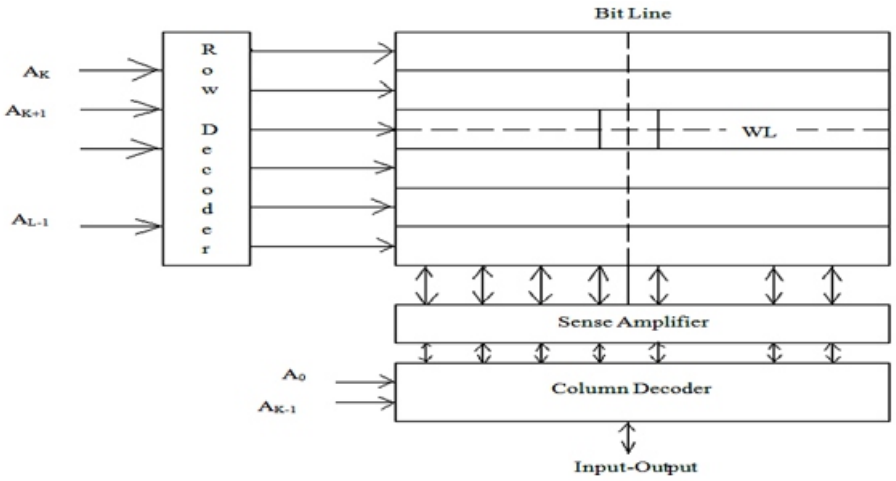


Fig. 1 Memory Architecture

DESIGN IMPLEMENTATION AND SIMULATION OF SENSE AMPLIFIERS

On the modern trends quick memories are highly required with low power consumption. The low power and low voltage CMOS techniques were applied extensively in analog and mixed mode circuits for the compatibility with the present IC technologies. Low power consumption can be achieved by using sense amplifiers which are main part of CMOS memory. Parasitic capacitance is much higher if memory is of high density. The large capacitance is an issue to make our each cell more energy to charge means low to sense amplifier. To achieve a faster memory and less power dissipation we have to design sense amplifiers as. Increase in number of cells per bit line which will increase the parasitic capacitance. Minimize supply voltage lead to short noise margin that affects the senseamplifier reliability. To maintain small voltage swing over the bit line, increase the area of each cell for design more memory on the chip which decreased the load on bit line. The wide range of applications of sense amplifier as it provides a photovoltaic system which usually stores enough energy for uncertainty in availability of solar radiation due statically nature of biosphere. These typical ICs are the complex component to measure the charge battery and discharge current. sense amplifiers plays a very smart role to maintain the reliability , accuracy and extended battery life by cutting power down over certain region to control heat. Mainly two types of SRAM sense amplifier linear amplifier and latch type amplifier.

As previously discussed in chapters about various sense amplifiers, it is found that some sense amplifier consume less power but with more delay than other consume slightly more power but speed (with less delay) is relatively large. In this dissertation I propose a new sensing scheme which has less delay, more sensitivity than previously discussed with less power consumption. This chapter divided into four parts.

- Current latch sense amplifier
- Latch operation
- The Sizing Consideration
- Body-biased controlled Current latch sense amplifier

These sense amplifiers made using with the help of Tanner tool V13.1.

CURRENT LATCH SENSE AMPLIFIER (CLSA)

Latch-type sense amplifiers, or sense amplifier based flip-flops, are very effective comparators. They achieve fast decisions due to a strong positive feedback and their differential input enables a low offset. The sense amplifiers circuit is the heart of memory.

The sense amplifiers are mainly designed to read the memory contents and amplify them to proper level using at logic circuits around memory. Sense amplifiers (SA) are hence widely applied in, for example, memories, A/D converters, data receivers and lately also in on-chip transceivers have become especially popular because of their high input impedance, full- swing output and absence of static power consumption. A good SA has the following properties namely, minimum sense delay, minimum power consumption, proper gain for amplification, minimum layout area, highly reliable, less number of cascading of transistors from source voltage to ground for low voltage operation and tolerable to environment. Thiskind of sense amplifier circuit is designed for increased speed, sensitivity with reduced power consumption. This design combines aspects from the latch based voltage mode sense amplifier and the differential Current Latch Sense Amplifier is based on voltage mode sense amplifier. It is also classified in differential type voltage sense amplifier. In this amplifier two cross-coupled inverters are used which give positive feedback as in latch type sense amplifier. But here the bitline is isolated from its output by using extra two nMOS transistors. So it has very high input impedance. The CLSA is shown in Fig 2

CIRCUIT CONFIGURATION

It consists of 5 nMOS and 4pMOS transistors namely MN1, MN2, MN3, MN4, and MN5.

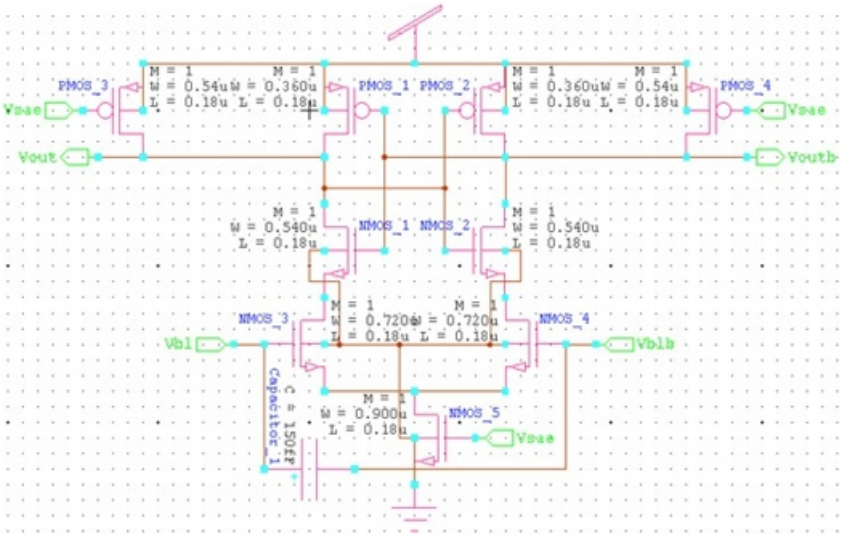


Fig. 2 Current Latch Sense Amplifier (CLSA)

MN1, MP1, MN2 and MP2 make two inverters connected in cross coupled manner give positive feedback in circuit.MN3 and MN4 are used to couple bitlines to CLSA amplifier.MP3 and MP4 are precharge transistors. The capacitor C represents the column capacitance of bitlines for filling of SRAM in circuit. The sense amplifier has following ports namely Vsae, vout, voutb, bl, blb. The bl and blb are column bit lines of SRAM. The signals are given to the **Vsae** which control the precharge and enable CLSA. The amplified output is taken from **Vout** node and complimentary output at **Voutb** node.

WORKING OF CURRENT LATCH SENSE AMPLIFIER (CLSA)

The sense amplifier is pre-charged in other words it is reset before sensing the bitlines. This action clears the previously latched data and charged the output nodes to the supply voltage. When the control signal **Vsae**, is at 0 logic means (low voltage) the pre-charge transistor MP3 and MP4 turned on so the output nodes are charged to supply voltage V_{DD}. When the sense amplifier enable signal Vsae is at high, the precharged transistors MP3 and MP4 turned off. But at this time transistors MN5 turned on so the drain of MN5 is pulled down to ground level. Due to this now, transistors MN3 and MN4 are working as a common source differential amplifier.

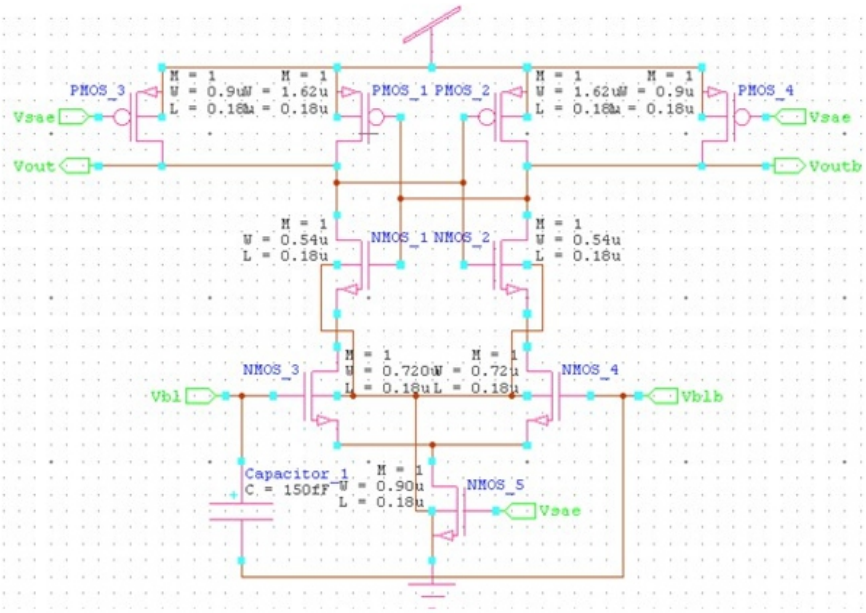


Fig. 3 Current Latch Sense Amplifier (CLSA) with different W/L ratio

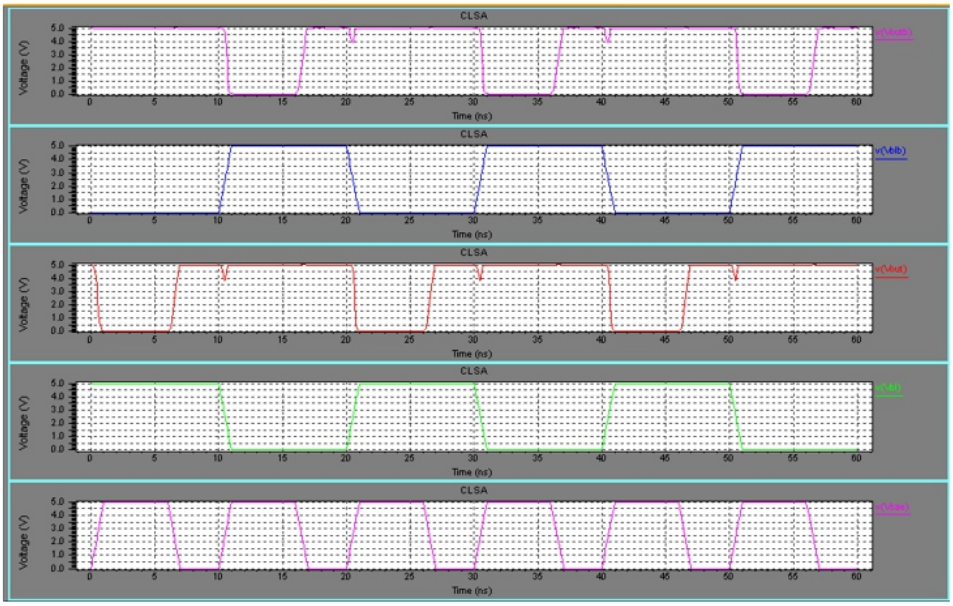
Due to the voltage difference developed by bit lines, bl and blb is transferred to drain nodes of transistors by the common source differential amplifier. At this time Vout and Voutb starts discharging suppose bl at V_{DD} and blb at V_{DD}-ΔV volts. This result gives more current flow thru MN3 than MN4.Due to this **Vout** node discharged rapidly than **Voutb**. Because out node rapidly discharging, when it reach at enough low level of voltage at this time the MN2 starts to on state. So the very high positive feedbacks loop work very inventively. This action causes outb node charged to V_{DD} level and out node to ground GND. Here transistor MN5 works as current source and transistor MN1, MP1, MN2 andMP2 work as latch and produce very high gain due to positive feedback. The speed of sense amplifier is depends on the how fast output nodes get charged thru pre-charging transistors. So by proper design pre-charge time kept as small as possible. CLSA performed sensing and amplification using without any current from bitlines to outputs so the sense and pre-charge power dissipation can bereduced. The main drawback is that it use 4 stages of transistor cascaded from V_{DD} to GND. It give results that CLSA not work at very low voltage due to very low differential current so speed is slow at low $V_{DD.}$

RESULT ANALYSIS AND COMPARISON

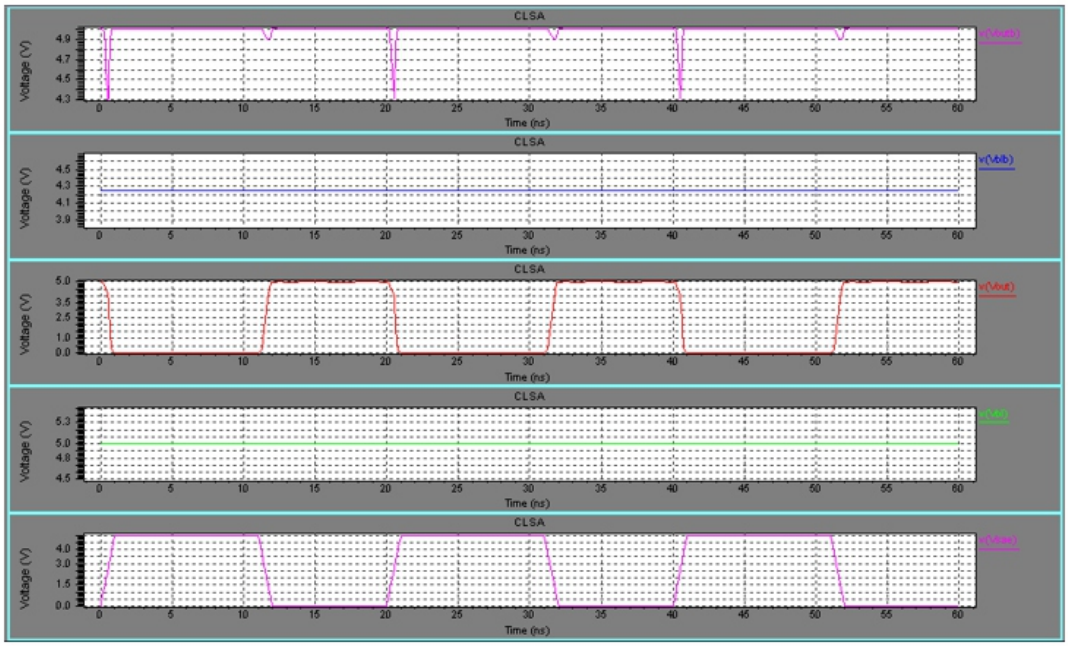
In this chapter here we show that the Simulation results of all implemented sense amplifiers. Function of designs is verified by using simulated based verification. This verification ensures that the design is functionally correct when tested with given set of inputs. Designed sense amplifiers have been implemented and simulated on Tanner tool in 180nm technology.

Current Latch Sense Amplifier (CLSA)

In this section I show the simulation results of Current Latch Sense Amplifier (CLSA). The simulation time is taken for CLSA amplifier is 60 neno seconds. The simulation waveform of the CLSA is shown in figure 5.1. Figure 5.1(a) shows the simulation waveform of the CLSA at V_{DD}=5Volt. V_{sae} given in pulses of 0.5 duty cycle with time period of 10n seconds both rise and fall time is 1n seconds. Similarly bit input to V_{bl} is in bit form and in sequence of 10101 and inverse of this is $V_{blb.}$ The total simulation time is 60n seconds.



(a)



(b)

Fig.4 Simulation waveforms of the Current Latch Sense Amplifier (CLSA) (a) for Bit Voltage (b) For Constant Voltage Difference

Similarly figure 5.1(b) shows the wave form at VDD at 5 volts, Vbl at 5 volts and Vblb taken at volts. The functionally this is shown in waveform that when Vsae is at low volts seen in v (Vase), the amplifier pre-charged to VDD. When Vsae is at high level then sense amplifier is in sensing mode so Vout should be 0volt if Vbl is at 5volt otherwise if Vblb is at 5 volts its value at full swing value which is 5volts. We obtained reverse value for Voutb node which is shown as Voutb value.

Table 1 CLSA operation

Vsae	Vbl	Vblb	Vout	Voutb	Remark
5V	5V	4.5 V	0V	5V	In sense mode
0V	5V	4.5 V	5V	5V	In pre-charge mode
5V	4.5V	5 V	5V	0V	In sense mode
0V	4.5V	5 V	5V	5V	In pre-charge mode

This is also true for pulse inputs.

Power dissipation of CLSA

The figure 4 shows the power dissipated by the Current Latch Sense Amplifier at VDD equal to 3V. This dissipation is measured for 100n seconds.

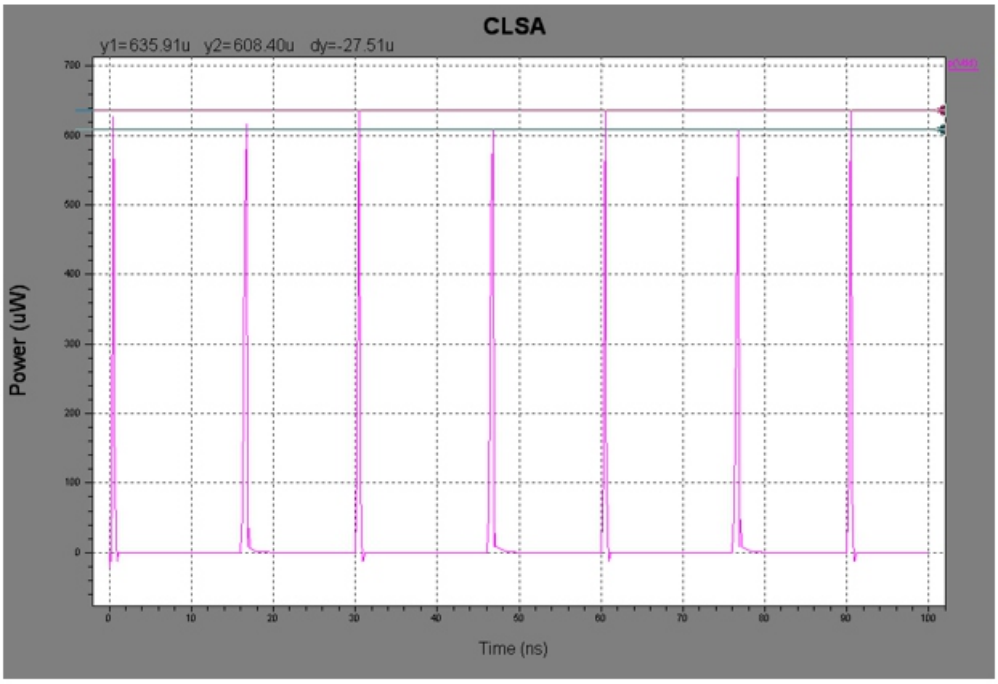


Fig. Simulation waveform of power dissipation of CLSA

Table 2 V_{DD} versus Pre-Charge Delay, Power Dissipation and Noise Margin of BB-CLSA

V_{DD} (V)	Pre-Charge Delay (ps)	Power Dissipation (µW)	Noise Margin V_{IL} (V)	Noise Margin V_{IH} (V)
5V	179	120.505	1.825	2.64
4 V	211.13	74.045	1.315	2.06
3 V	221.98	28.13	0.680	1.51
2 V	241.04	12.695	0.605	1.055
1 V	467.59	5.25	0.436	0.628

CONCLUSION AND FUTURE SCOPE

Conclusion

In this dissertation Body Bias Controlled Current Latch Sense Amplifier has been designed and simulated using 180nm CMOS technology of tanner tool at a various supply voltage from1.0V to 5.0V. A Sense Amplifier is specially proposed in this dissertation as it is the heart of the Memory. Especially I proposed a BB-CLSA for low power and high speed operations in SRAM. This proposed Sense amplifier is compared with nearest basic Current Latch Sense amplifier as

- The power consumption of proposed BB-CLSA has been reduced from 47% to 87% compared to conventional CLSA.
- Speed of proposed Sense amplifier is increased by 10% as compared to conventional CLSA.
- Noise Margin and Sensitivity of proposed sense amplifier is improved considerably.
- Body Bias method is used for high speed at low power dissipation operation.
- Only 44% more transistors are used to reduce about 87% power dissipation and to get 10% more high speed operation.

Future Scope

However some aspects of the goal have been achieved using this design, but still a better Sense Amplifier can be build by some improvement in the circuit design. The SA can be further extended and modified by the following points.

- Delay can be further reduced by improving circuit design.
- Affect of process variations and corner variations on the performance of the proposed sense amplifiers are not included. So effects of these variations are removed by proper design of circuits and accurate simulations.
- Yield measurements can be done
- The layout can also be designed using L-Edit of tanner tool by which area can be calculated for chip fabrication.
- Body Bias Voltage Latch Sense amplifier is designed for high speed operation.
- In this design we use 180 nm technologies but latest technology 28nm and more can be used for batter design and analysis.
- The layout can also be designed using L-Edit of tanner tool by which area can be calculated for chip fabrication
- The delay and power dissipation can also reduced by using low power and high speed techniques like VTCMOS, DTCMOS, and Adaptive CMOS and Adiabatic logic technology.

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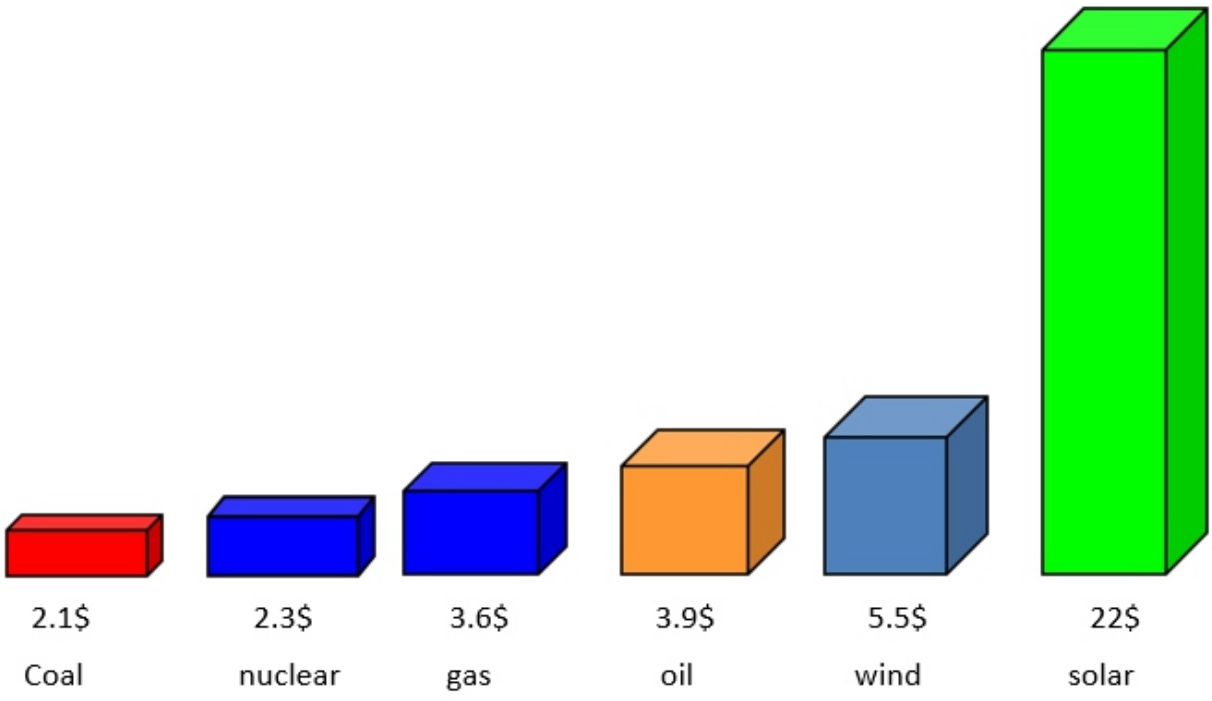

2.1$
Coal
2.3$
nuclear
3.6$
gas
3.9$
oil
5.5$
wind
22$
solar

In order to overcome such high costs solar cell must either be made from cheaper material or become more efficient. The region between 400nm and 1100nm has the highest photon density in the am 1.5 solar spectrum. A material that cans absorb sunlight between 400nm and 1100nm would be the ideal absorber. Silicon and multijunction solar cells are very efficient at converting sunlight to electricity but they are competitive in price to fossil fuels.

A promising alternative to silicon and multijunction solar cells are dye sensitized solar cells (DSSC). DSSC have the potential to be as efficient as silicon solar cells, but at a fraction of the cost of silicon and multjunction solar cells.

The efficiency (Ƞ) of a DSSC is determined by the ratio of the power of the DSSC (PDSSC) to the power of incident light (Pin).The power of DSSC is determined by the short circuit current density (Jsc) open circuit voltage (voc) and fill factor (FF). The short circuit current density is given by the current measured at short circuit conditions or the current measured when there is zero applied voltage. The open circuit voltage is the voltage measured when the cell is at open circuit or the voltage that is applied to produce zero current. The fill factor is simply the ratio of the measured power of the solar cell from the current voltage curves to the maximal theoretical power of the solar cell. If recombination is high then the fill factor will be low and if there is little to no recombination the FF will be near unity, but in efficient solar cells the FF is 0.6 -0.8. It can be concluded that by increasing the Jsc, Voc or FF one can increase the Ƞ

Ƞ=PDSSC/Pin
=Jsc Voc FF/Pin

Consolidated tables showing an extensive listing of the highest independently confirmed efficiencies for solar cells and modules are presented. Highest confirmed "one-sun" cell and module results are reported in table I and II. Table I summarizes the best measurements for cells and sub modules, while Table II shows the best results for modules. The most important criterion for inclusion of results into the tables is that they must have been measured by a recognized test centre. A distinction is made between three different eligible areas: total area; aperture area and designated illumination area.

Table I. confirmed terrestrial cell and sub module efficiencies measured under the global AM1.5 spectrum (1000W/m ^{2}) at 25^0 C

Classification *Test Centre*[e]	*Effic.*[b] *(%)*	*Area*[c] *(cm^2)*	*V_{oc}* *(v)*	*J_{sc}* *(mA/cm^2)*	*FF*[d]	*(and*
Data)						
Silicon						
Si (crystalline)	25.0±0.5	4.00(da)	0.706	42.7	82.8	Sandia
Si (multicrystalline)	20.4±0.5	1.002(ap)	0.664	38.0	80.9	NREL
Si (thin film transfer)	16.7±0.4	4.017(ap)	0.645	33.0	78.2	FhG-ISE
Si (thin film sub module)	10.5±0.3	94.0(ap)	0.492	29.7	72.1	FhG-ISE
GaAs (thin film)	27.6±0.8	0.9989(ap)	1.107	29.6	84.1	NREL
GaAs (multicrystalline)	18.4±0.5	4.011(t)	0.994	23.2	79.7	NREL
InP (crystalline)	22.1±0.7	4.02(t)	0.878	29.5	85.4	NREL
Thin Film Chalcogenide						
CIGS (cell)	19.6±0.6	0.996(ap)	0.713	34.8	79.2	NREL
CIGS (sub module)	16.7±0.4	16.0(ap)	0.661	33.6	75.1	FhG-ISE
CdTe (cell)	16.7±0.5	1.032(ap)	0.845	26.1	75.5	NREL
CdTe (sub module)	12.5±0.4	35.03(ap)	0.838	21.2	70.5	NREL
Amorphous/nanocrystalline Si						
Si(amorphous)	10.1±0.3	1.036(ap)	0.886	16.75	67	NREL
Si(nanocrystalline)	10.1±0.2	1.199(ap)	0.539	24.4	76.6	JQA
Photochemical						
Dye sensetised	10.4±0.3	1.004(ap)	0.729	22	65.2	AIST
Dye sensetised (sub module)	9.9±0.4	17.11(ap)	0.719	19.4	71.4	AIST
Organic						
Organic polymer	8.3±0.3	1.031(ap)	0.816	14.46	70.2	NREL
Organic (sub module)	3.5±0.3	208.4(ap)	0.847	8.62	48.3	NREL
Organic (2-cell tandem)	8.3±0.3	1.087(ap)	1.733	8.03	59.5	FhG-ISE
Multijunction devices						
GaInP/GaAs/Ge	32.0±1.5	3.989(t)	2.622	14.37	85	NREL
GaAs/CIS(thin film)	25.8±1.3	4.00(t)	-	-	-	NREL
a-Si/µc-Si(thin film cell)	11.9±0.8	1.227	1.346	12.92	68.5	NREL
a-Si/µc-Si(thin film sub module)	11.7±0.4	14.23(ap)	5.462	2.99	71.3	AIST

a
CIGS =CuInGa2; a-Si= amorphous silicon/ hydrogen alloy

b
Effic.=efficiency

c
(ap)=aperture area; (t)=total area; (da)=designated illumination area

d
FF=fill factor

E
FhG-ISE=Fraunhofer Institute for Solar Energiesysteme; JQA= Japan Quality Assurance; AIST=Japan

Table II. Confirmed terrestrial module efficiencies measured under the global AM1.5 spectrum (1000W/m ^{2}) at 25^0 C

Classification	*Effic .[b] (%)*	*Area [c] (cm^2)*	V_{oc} *(v)*	I_{sc} *(A)*	FF[d]	*Test Centre (and Data)*
Si (crystalline) Sandia	22.9±0.6	778(da)	5.6	3.97	80.3	
Si (large crystalline)	21.4±0.6	15780(ap)	68.6	6.293	78.4	NREL
Si (multicrystalline)	17.55±0.5	14701(ap)	38.31	8.94	75.3	ESTI
Si (thin film polycrystalline) Sandia	8.2±0.2	661(ap)	25	0.32	68	
CIGS	15.7±0.5	9703(ap)	28.24	7.254	72.5	NREL
CIGSS (Cd free)	13.5±0.7	3459(ap)	31.2	2.18	68.9	NREL
CdTe	10.9±0.5	4874(ap)	26.21	3.24	62.3	NREL

This context is focused on liquid redox electrolytes in dye – sensitized solar cells (DSCS). A liquid redox electrolyte as one of the key constitutes in DSCS typically consists of a redox mediator, additives and a solvent.

DEVELOPMENT OF SOLAR CELLS

Solar cells are electrical devices that directly convert sunlight into electrically. Since the modern discovery of the silicon p-n junction PV devices (Solar Cells) , the global PV industry has experienced revolutionary developments and market growth. The solar industry has been the fastest growing renewable energy technology in recent years.

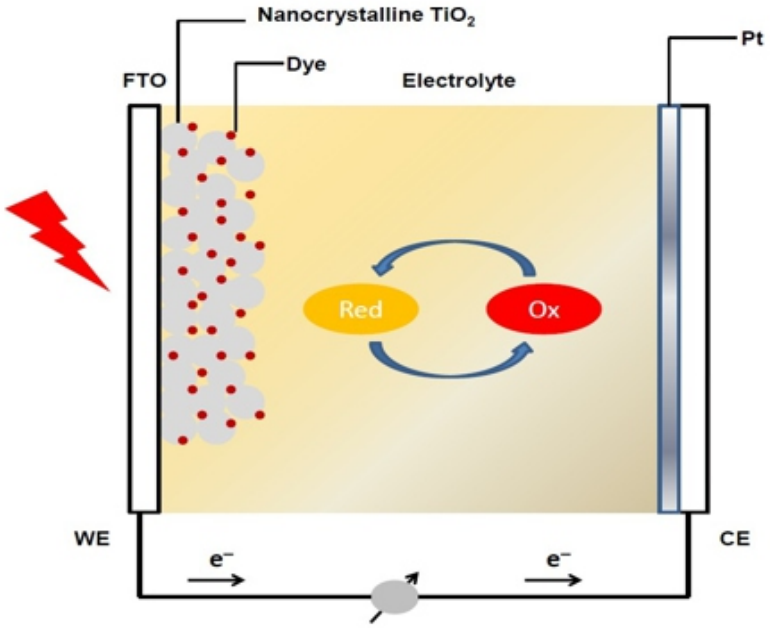
The first generations of solar cells from industrialization point of view are based on crystalline silicon. The manufacture of silicon – based solar cells involves high purity silicon, the manufacturing processes of which are extremely expensive. The high cost of the generation solar cells severely restricts their widespread application in the future.

The second generations of solar cells are normally referred to as thin film solar cells. Amorphous silicon , Cadmium telluride(CDTE) , Copper indium gallium selenide (CIGS) are the three most commonly used materials for the second generation solar cells to use far less materials required in a solar cells , which significantly reduce the production cost in contrast to the first generation solar cells are lower than the first generation solar cells.

Dye – sensitized solar cells were significantly improved in 1991. In contrast to conventional systems where the semiconductor takes both the function of light absorption and charge career transport, these two functions are separated in DSCs. The light absorption is performed by a monolayer of dye molecules attached to a mesoporous layer of a wide band gap semiconductor. Charge separation takes place at the semiconductor/dye interface. Charge carriers are transported in the conduction band edge (CB) of the semiconductor to the charge collector. DSCs are considered to be a technology between the second and third generation solar cells.

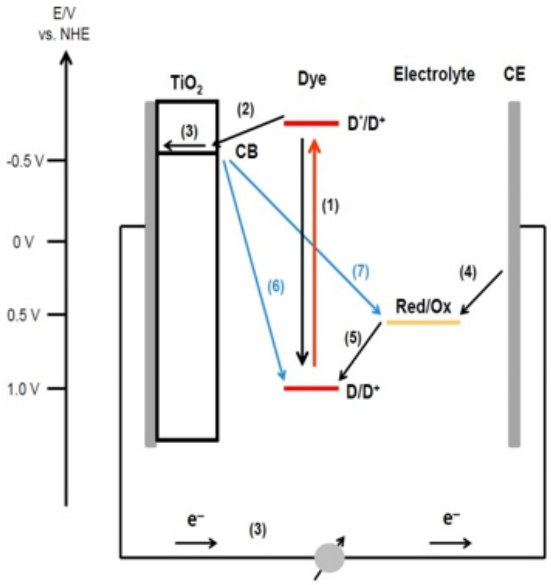
DYE-SENSITIZED SOLAR CELLS (DSCS)

DSC consists of three major components: semiconductor, sensitizer and electrolyte between two electrodes. The device generates electric power without suffering any permanent chemical transformation.



Schematic structure of a DSC

Working electrodes consists of a mesoporous layer of metal oxide semiconductor typically TIO_2, screen printed onto the conducting glass substrates, typically fluorine-doped tin oxide. The nanoparticle size is around 20 nm in diameter and typical film thicknesses are 10 μm. Liquid electrolytes consists of a redox couple and additives dissolved in a liquid solvent. Counter electrodes are prepared by depositing a thin layer of Platinum catalyst onto the fluorine-doped tin oxide.

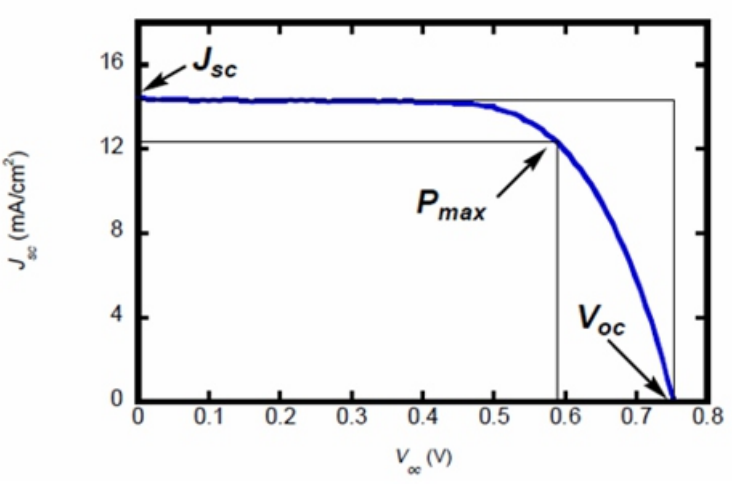


Operation principle in DSCs

Upon light irradiation, the monolayer of the sensitizer is photo excited. The excited electrons are injected into the conduction band in the TIO_2. The electrons penetrate throughthe nanocrystalline TIO_2 film to the back contact of the conducting substrate and flow through an external circuit. The photovoltaic performance of liquid electrolyte- based DSCs depend strongly on the choice of electrolyte solvent. Organic solvent and ionic liquids are two major types of liquid electrolyte solvents.

A redox couple is the key component in a liquid electrolyte, assuming the tasks for dye regeneration and charge transport between the two electrodes, playing a circuit role in determining the photovoltaic performance of DSCs. Iodine/ triiodide has been used as a redox couple from the very beginning of DSC research. Organic sensitizes have attracted much attention in recent years due to their advantages, high molecular extinction coefficients, which allow DSCs to use thinner layer of TIO_2 film , thus leading to the improvements of charge collection efficiency. In addition to a redox couple , various additives i.e. specific cations or or compounds , are normally introduced into the liquid electrolytes. Two kinds of additives are typically employed in liquid electrolytes for DSCs. One class of additives in liquid electrolytes incorporates specific cations such as alkali cations or guanidium cations .Nitrogen –containing heterocyclic compound , such as 4-tert- butylpyridine is another class of the most frequently used additives .

Current – voltage measurement is the most important and conventional technique for the assessment of the photovoltaic performance. The most important photovoltaic parameter to evaluate the performance of DSC devices is the overall light-to-electricity conversion efficiency (Ƞ) , which is determined by the product of the short-circuit current density(Jsc), open –circuit voltage(Voc) and fill factor(FF) divided by the intensity of the incident light(Pin).

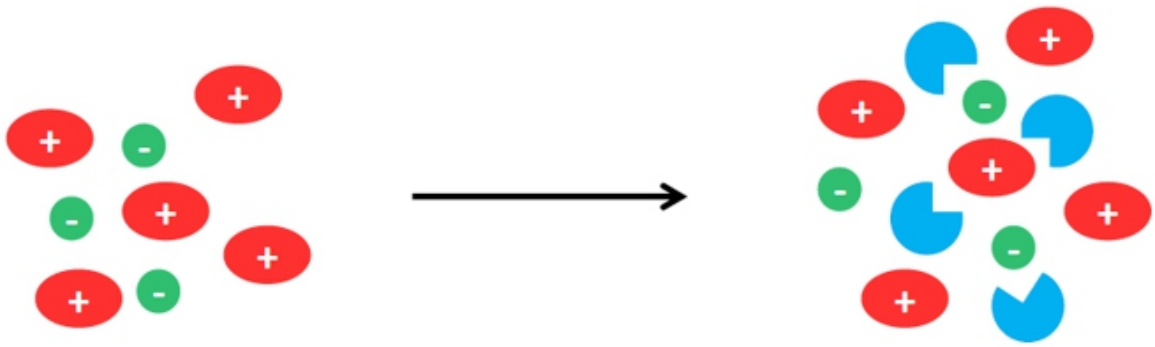


I-V characteristics of a DSC device

FF=Pmax/Jsc.Voc

η=Jsc.Voc.FF/Pin

Incompletely Solvated Ionic Liquids as Electrolyte Solvents



Mixtures between ionic liquids and molecular solvents exhibit interesting physical and chemical properties that deviate from their parent components. At low concentrations or molar ratios of the molecular solvent, the mixture in most aspects chemically behaves like an ionic liquid as long as the number of solvent molecules are insufficient to fully solvate the ions of the salt.

CONCLUSIONS

The influences of different cations of lithium, sodium and guanidinium in the electrolytes on the photovoltaic characteristics for DSCs have been investigated. Upon addition of cations into the reference electrolyte, short-circuit currents are all found to be significantly enhanced, largely due to the positive shift of the CB in the TiO2, probably resulting in an increase of the electron injection yield from the excited state of the sensitizing dye to the CB of TiO2. Different behaviors in the photovoltages are

are observed for different cations. The optimal overall conversion efficiency is obtained by the electrolyte with additional guanidinium cations, benefiting from the dual gains of both short-circuit current and open- circuit voltage relative to the reference electrolyte.

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Implementation of Incremental Conductance (Mppt) Technique For PV System

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A B S T R A C T

This project investigates in detail the concept of Maximum Power Point Tracking (MPPT) which significantly increases the efficiency of the solar photovoltaic system. The project proposes a simple MPPT algorithm is called Incremental conductance Method. This method computes the maximum power and controls directly the extracted power from the PV. The proposed method offers different advantages which are: good tracking efficiency, response is high and well control for the extracted power. The resultant system is capable of tracking MPPs accurately and rapidly without steady-state oscillation, and also, its dynamic performance is satisfactory. First the photovoltaic module is analyzed using SIMULINK software. The main aim will be to track the maximum power point of the photovoltaic module so that the maximum possible power can be extracted from the photovoltaic. For the main aim of the project Maximum Power Point Tracking control mechanism is used. Modeling the converter and the solar cell in Simulink and interfacing both with the MPPT algorithm to obtain the maximum power point operation would be of prime importance A MPPT plays a very vital role for extracting the maximum power from the solar PV module and transferring that power to the load. Modeling the converter and the solar cell in Simulink and interfacing both with the MPPT algorithm to obtain the maximum power point operation would be of prime importance.

Keywords: maximum power point tracking, photovoltaic cell, cuk converter, buk converter

I. INTRODUCTION

Global warming and energy policies have become a hot topic on the international agenda in the last years. Developed countries are trying to reduce their greenhouse gas emissions. For example, the EU has committed to reduce the emissions of greenhouse gas to at least 20% below 1990 levels and to produce no less than 20% of its energy consumption from renewable sources by 2020 [1]. In this context, photovoltaic (PV) power generation has an important role to play due to the fact that it is a green source. The only emissions associated with PV power generation are those from the production of its components. After their installation they generate electricity from the solar irradiation without emitting greenhouse gases.

Tracking the maximum power point (MPP) of a photovoltaic (PV) array is usually an essential part of a PV system. Renewable sources of energy acquire growing importance due to its enormous consumption and exhaustion of fossil fuel. Also, solar energy is the most readily available source of energy and it is free. The rapid increase in the demand for electricity and the recent change in the environmental conditions such as global warming led to a need for a new source of energy that is cheaper and sustainable with less carbon emissions. Solar energy has offered promising results in the quest of finding the solution to the problem. A great deal of research has been done to improve the efficiency of the PV modules. A number of methods of how to track the maximum power point of a PV module have been proposed to solve the problem of efficiency and products using these methods have been manufactured and are now commercially available for consumers [5-7]. A MPPT is used for extracting the maximum power from the solar PV module and transferring that power to the load [2-3].

A dc/dc converter (step up/ step down) serves the purpose of transferring maximum power from the solar PV module to the load. A dc/dc converter acts as an interface between the load [3]. By changing the duty cycle the load impedance as seen by the source is varied and matched at the point of the peak power with the source so as to transfer the maximum power [3]. This manuscript steps through a wide variety of methods with a brief discussion and categorization of each. We have avoided discussing slight modifications of existing methods as distinct methods. Therefore MPPT techniques are needed to maintain the PV array's operating at its MPP [17]. Many MPPT techniques have been proposed in the literature; examples are the Perturb and Observe (P&O) methods, Incremental Conductance (IC) methods, Fuzzy Logic Method etc.

II. PV CELL MODELING

The solar cell is the basic unit of a PV system. An individual solar cell produces direct current and power typically between 1 and 2 W, hardly enough to power most applications. Solar Cell or Photovoltaic (PV) cell is a device that is made up of semiconductor materials such as silicon, gallium arsenide and cadmium telluride, etc. that converts sunlight directly into electricity. The voltage of a solar cell does not depend strongly on the solar irradiance but depends primarily on the cell temperature. PV modules can be designed to operate at different voltages by connecting solar cells in series. When solar cells absorb sunlight, free electrons and holes are created at positive/negative junctions. If the positive and negative junctions of solar cell are connected to DC electrical equipment, current is delivered to operate the electrical equipment.

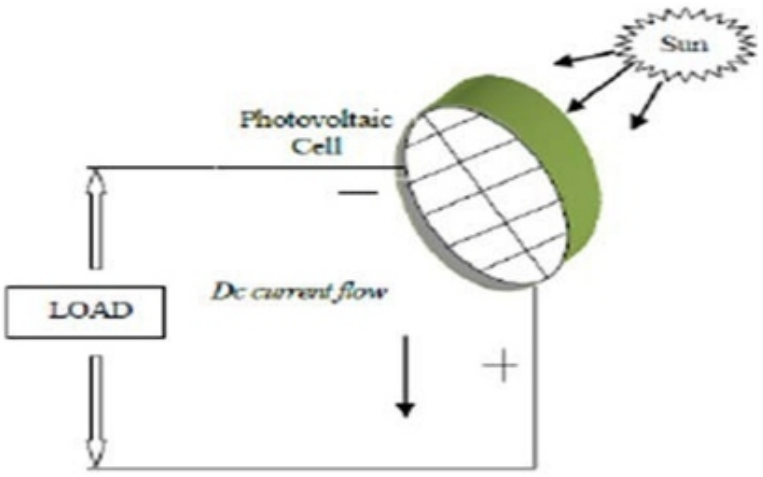

Fig 1: PV Cell

The positive and negative charges created by the absorption of photons are thus encouraged to drift to the front and back of the solar cell. The back is completely covered by a metallic contact to remove the charges to the electric load. The collection of charges from the front of the cell is aided by a fine grid of narrow metallic fingers. [5]The p-n junction provides an electrical field that sweeps the electrons in one direction and the positive holes in the other. If the junction is in thermodynamic equilibrium, then the Fermi energy must be uniform throughout. Since the Fermi level is near the top of the gap of an n-doped material and near the bottom of the p-doped side, an electric field must exist at the junction providing the charge separation function of the cell.

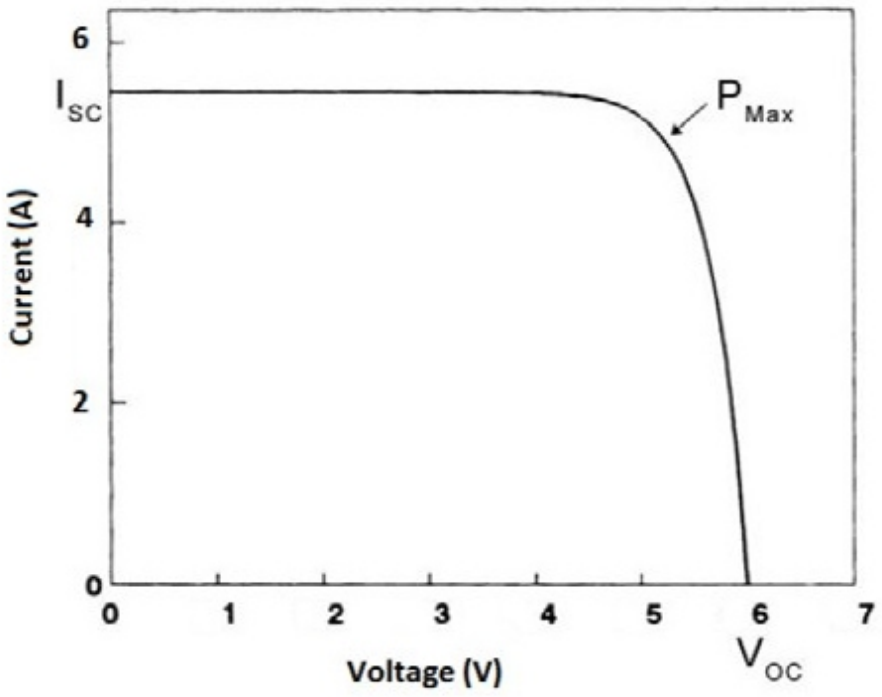

Fig 2: I-V characteristics of a solar panel

Three points in these curves are of particular interest: 1. Short circuit point, where the voltage over the module is zero and the current is at its maximum (short circuit current *Isc*).

2. Maximum power point or MPP, where the product of current and voltage has its maximum (defined by *Impp.Vmpp*). 3. Open circuit point, where the current is zero and the voltage has its maximum (open circuit voltage *Voc*). The measurements taken for obtaining an *I-V* curve is done by controlling the load current. At open circuit, when no load current is generated, a first characteristic value can be measured: the open circuit voltage *Voc*. Increasing the load fed by the photovoltaic module leads to a decreasing voltage *V* with an increasing current *I*. In other words, by increasing the load current from zero to its maximum value, the operating point moves from the open circuit voltage at zero current to the short circuit current *Isc* at zero voltage. The series of all measured pairs (*V*, *I*) yields the characteristic *I-V* curve of the module. From the characteristic curve of the module, it is clear that the open circuit voltage of the photovoltaic module, the point of intersection of the curve with the horizontal axis, varies little with solar radiation changes. It is inversely proportional to temperature, i.e., a rise in temperature produces a decrease in voltage. Short circuit current, the point of intersection of the curve with the vertical axis, is directly proportional to solar radiation and is relatively steady with temperature variations. Actually, the photovoltaic module acts like a constant current source for most parts of its *I-V* curve

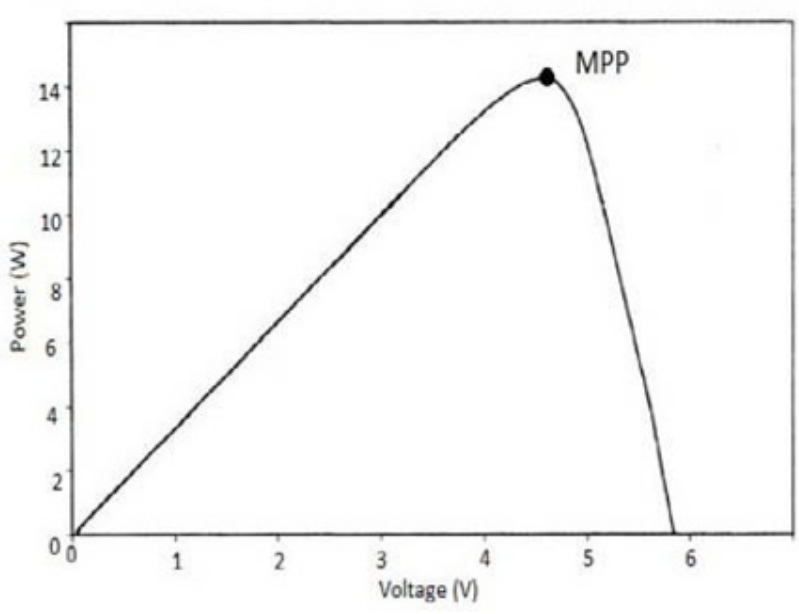

Fig 3: P-V characteristics of a solar panel

This is the P-V characteristics of PV cell. When the voltage and the current characteristics are multiplied we get the P-V characteristics as shown in fig.4 The point indicated as MPP is the point at which the panel power output is maximum.

III. MAXIMUM POWER POINT TRACKING

Maximum Power Point Tracking, frequently referred to as MPPT, is an electronic system that operates the Photovoltaic (PV) modules in a manner that allows the modules to produce all the power they are capable of. MPPT is not a mechanical tracking system that "physically moves" the modules to make them point more directly at the sun[17] . MPPT is a fully electronic system that varies the electrical operating point of the modules so that the modules are able to deliver maximum available power. Additional power harvested from the modules is then made available as increased battery charge current. MPPT can be used in conjunction with a mechanical tracking system, but the two systems are completely different.

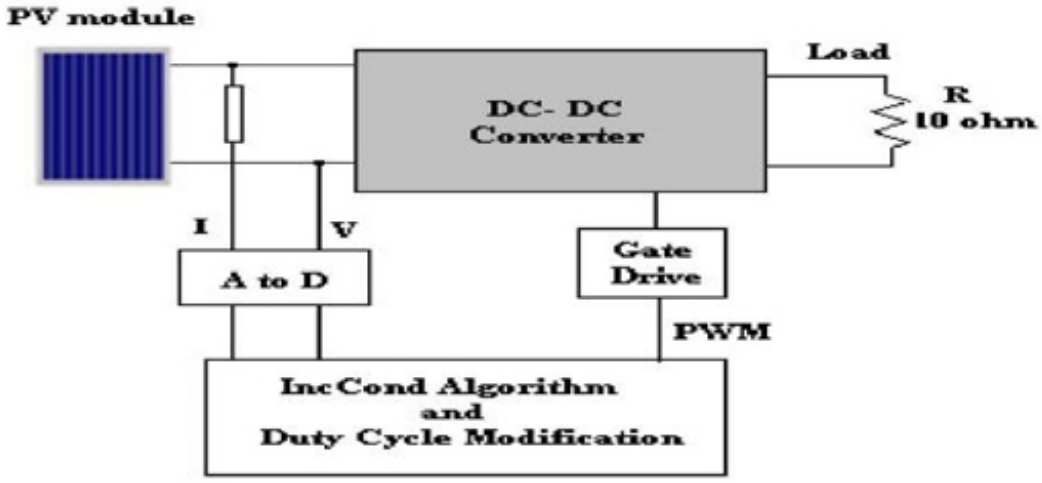

Fig 4: Block diagram of typical MPPT system

Solar panel is used as energy source. DC-DC Converter is used for transferring maximum power from the solar PV module to the load. MPPT Controller track maximum power.

Incremental conductance

The time complexity of perturb & observe algorithm is very less but on reaching very close to the MPP it doesn't stop at the MPP and keeps on perturbing on both the directions. When this happens the algorithm has reached very close to the MPP and we can set an appropriate error limit or can use a wait function which ends up increasing the time complexity of the algorithm. [5] However the method does not take account of the rapid change of irradiation level (due to which MPPT changes) and considers it as a change in MPP due to perturbation and ends up calculating the wrong MPP. To avoid this problem we can use incremental conductance method.

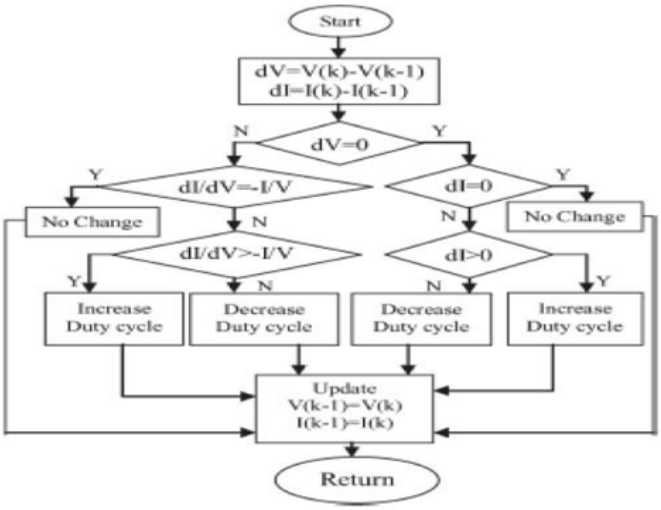

Fig 5: Algorithm for Incremental Conductance Method

The disadvantage of the perturb and observe method to track the peak power under fast varying atmospheric condition is overcome by IC method. The IC can determine that the MPPT has reached the MPP and stop perturbing the operating point. If this condition is not met, the direction in which the MPPT operating point must be perturbed can be calculated using the relationship between dl/dV and –I/V This relationship is derived from the fact that dP/dV is negative when the MPPT is to the right of the MPP and positive when it is to the left of the MPP. This algorithm has advantages over P&O in that it can determine when the MPPT has reached the MPP, where P&O oscillates around the MPP. Also, incremental conductance can track rapidly increasing and decreasing irradiance conditions with higher accuracy than P and O.[7,8]

This relationship is derived from the fact that

$$\frac{dI}{dV} = -\frac{I}{V}, \quad \text{at MPP}$$

$$\frac{dI}{dV} > -\frac{I}{V}, \quad \text{left of MPP}$$

$$\frac{dI}{dV} < -\frac{I}{V}, \quad \text{right of MPP}$$

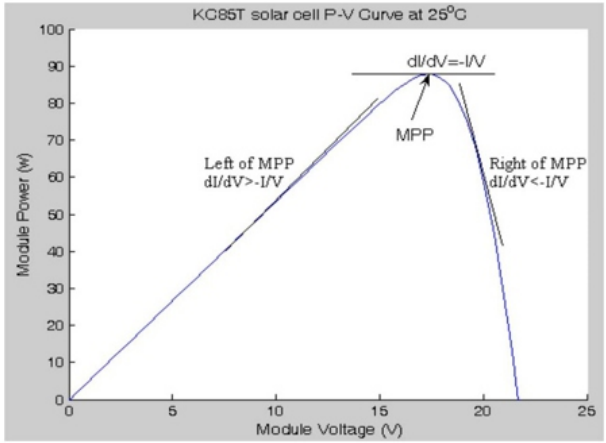

Fig 6: P-V characteristics for Incremental Conductance Algorithm

IV. CUK CONVERTER

The Cuk converter is obtained by using the duality principle on the circuit of a buck-boost converter. Similar to the buck-boost converter, the Cuk converter provides a negative polarity regulated output voltage with respect to the common terminal of the input voltage. The output voltage magnitude can be same, larger or smaller than the input, depending on the duty cycle. The inductor on the input acts as a filter for the dc supply, to prevent large harmonic content. Here, the capacitor C1 acts as the primary means storing and transferring energy from the input to the output.

The analysis begins with these assumptions:

1. Both inductors are very large and the currents in them are constant.
2. Both capacitors are very large and the voltages across them are constant.
3. The circuit is operating in the steady state, meaning the voltage and current waveforms are periodic.
4. For the duty ratio of D, the switch is closed for time DT and open for (1-D) T.
5. The switch and the diode are ideal.

In steady state, the average inductor voltages VL1 and VL2 are zero. Therefore by Figure 7

$$V_{C1}=Vs+V_{o} \qquad (1)$$

Therefore, VC1 is larger than both Vs and Vo. Assuming C1 to be sufficiently large, in steady state the variation in vC1 from its average value VC1 can be assumed to be negligibly small (VC1≈vC1), even though it stores and transfers energy from the input to the output.

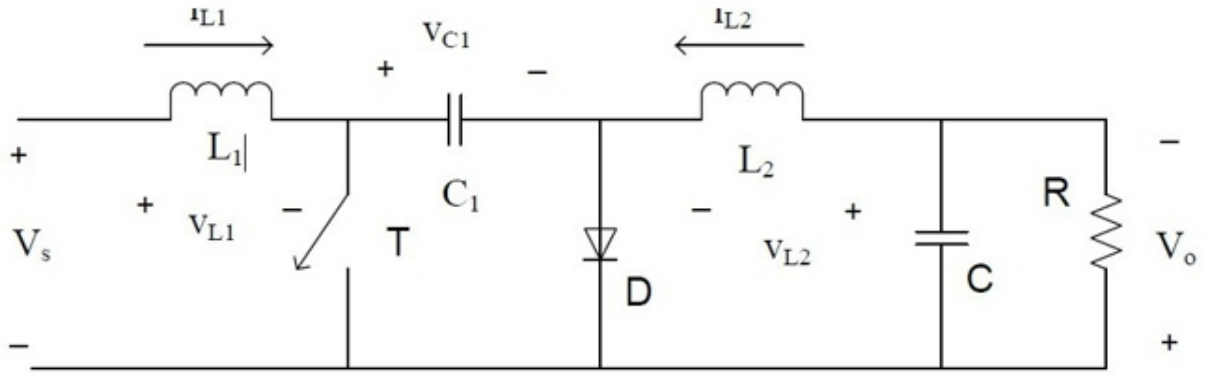

Fig 7: Circuit diagram of a Cuk converter

When the switch is off, the inductor currents iL1 and iL2 flow through the diode. Capacitor C1 is charged through the diode. The circuit is shown in Figure 7, Capacitor C1 is charged through the diode by energy from both the input and L1. Current iL1 decreases because VC1 is larger than Vs. Energy stored in feeds the output. Therefore iL2 also decreases.

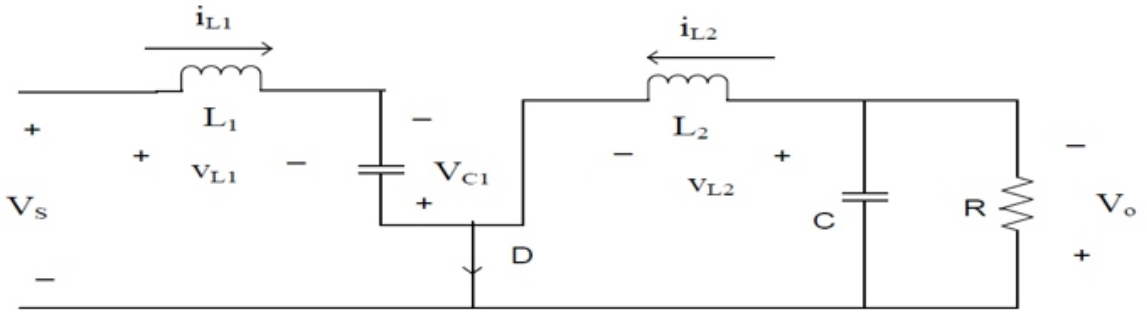

Fig 8: Voltage and Current in a Cuk converter with Switch Off

When the switch is on, VC1 reverse biases the diode. The inductor currents iL1 and iL2 flow through the switch as shown in Figure 8. Since VC1 >Vo, C1 discharges through the switch, transferring energy to the output and L2. Therefore iL2 increases the input feeds energy to L1 causing iL1 to increase.

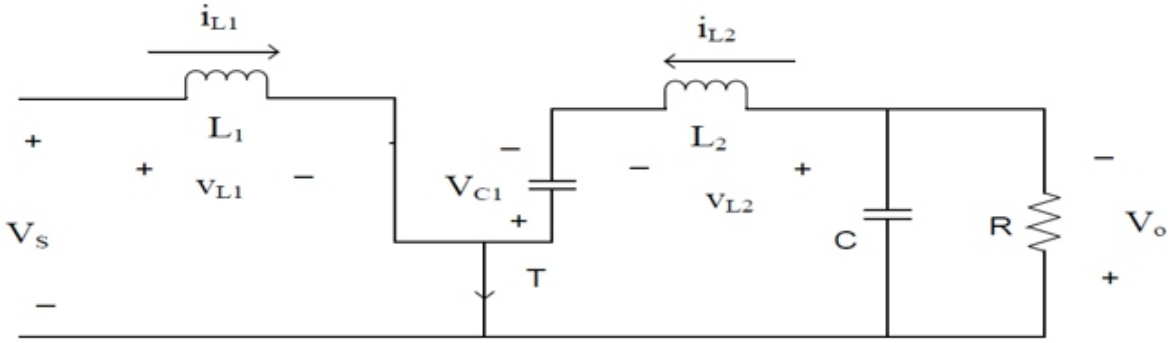

Fig 9: Voltage and Current in a Cuk converter with Switch On

The inductor currents iL1 and iL2 are assumed to be continuous. The voltage and the current expressions in steady state can be obtained in two different ways. If we assume the capacitor voltage VC1 to be constant, then equating the integral of the voltages across L1 and L2 over one time period to zero yields

L1: $V_sDT_s-(V_s-V_{c1})\ (1-D)\ T_s=0$ ----------(2)

L2: $(V_{c1}-V_0)\ DT_s + (-V_0)\ (1-D)\ T_s = 0$----------(3)

$V_{c1}= (1/1-D)*V_s$ ----------(4)

$V_{c1} = (1/D)*V_0$ ----------(5)

From equation (4) and (5) we get,

$V_0/V_s = (D/1-D)$ ----------(6)

Next, the average power supplied by the source must be same as the average power absorbed by the load.

$P_s = P_0$

$V_s I_{L1} = V_0 I_{L2}$ ----------(7)

$I_{L1}/I_{L2} = V_0/V_s$ ----------(8)

$I_0/I_s = (1-D)/D$ ----------(9)

Benefits:

1. An advantage of this circuit is that both the input current and the current feeding the output stage are reasonably ripple free. It is possible to simultaneously eliminate the ripples in iL1 and iL1 completely, leading to lower external filtering requirements.

2. This converter is also able to step up and down the voltage. It uses a capacitor as the main energy storage. As a result, the input current is continuous.

3. This circuit has low switching losses and high efficiency.

4 This converter does not allow electromagnetic interference like others.

Drawbacks:

1. A significant disadvantage is the requirement of a capacitor C1 with a large ripple current-carrying capability.

2. In practical circuits, the assumption of a nearly constant is reasonably valid.

3. Its relationship to the duty cycle (D) is:

If $0 < D < 0.5$ the output is smaller than the input.

If $D = 0.5$ the output is the same as the input.

If $0.5 < D < 1$ the output is larger than the input.

V. SIMULINK MODEL

Simulink model for Cuk Converter Circuit

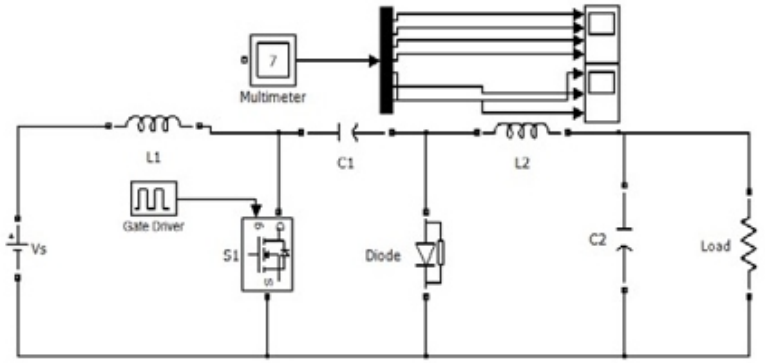

Fig 10: Cuk Converter

Simulink model for PV System Circuit

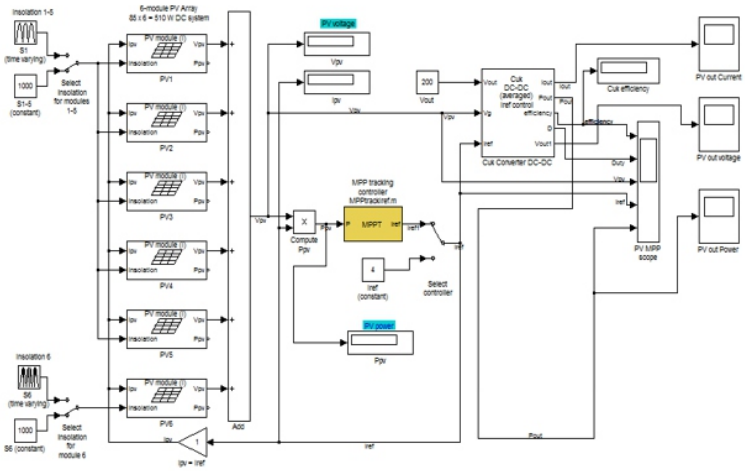

Fig 11: Simulink model for PV System Circuit

RESULTS

O/P of Cuk Converter

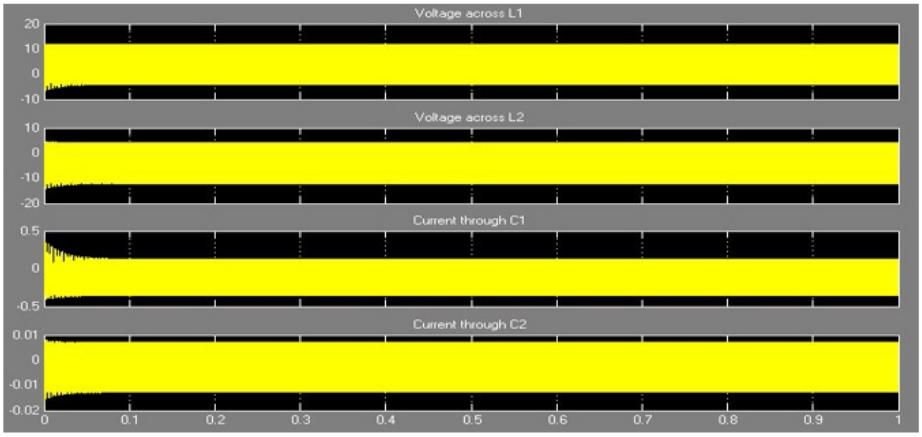

Fig 12 : O/P of Cuk Converter 1 with 25% duty cycle

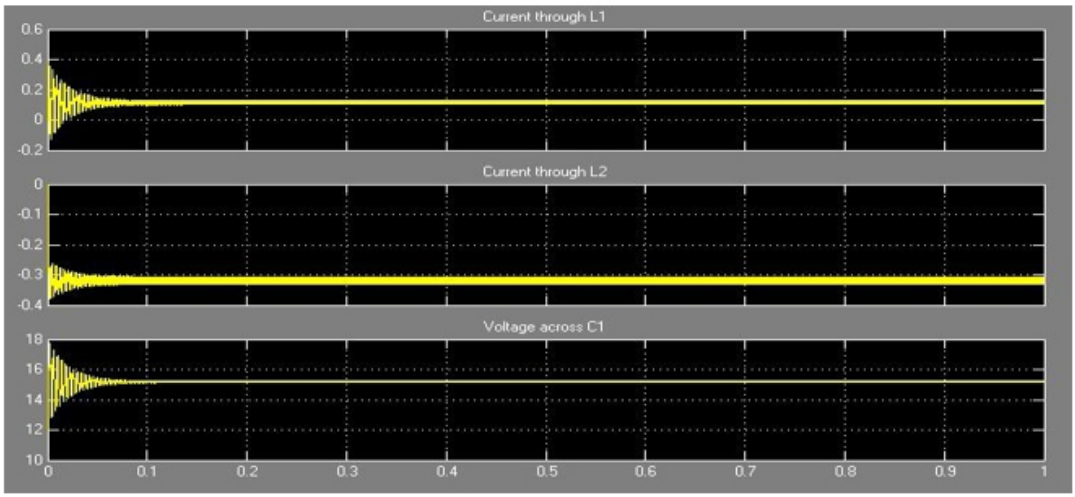

Fig 13: O/P of Cuk Converter 2 with 25% duty cycle

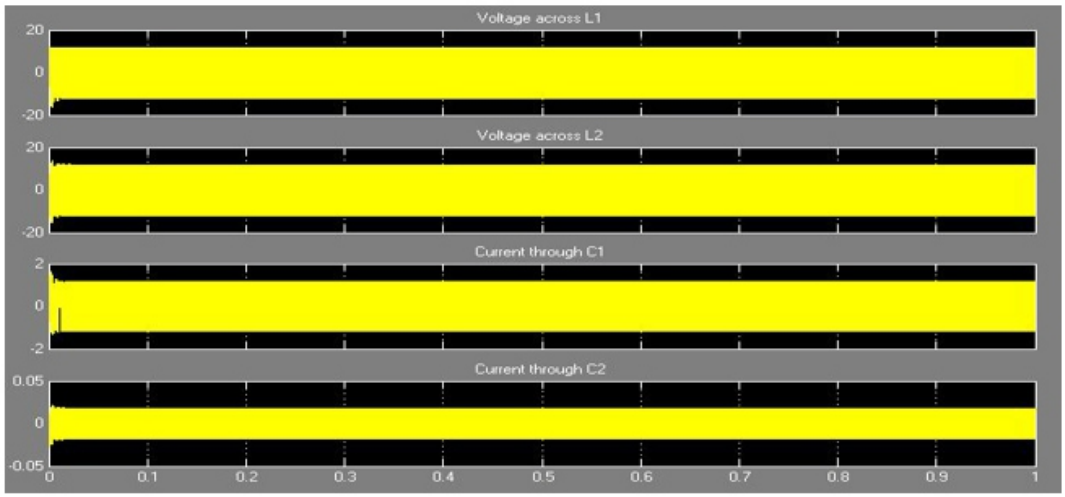

Fig 14: O/P of Cuk Converter 1 with 50% duty cycle

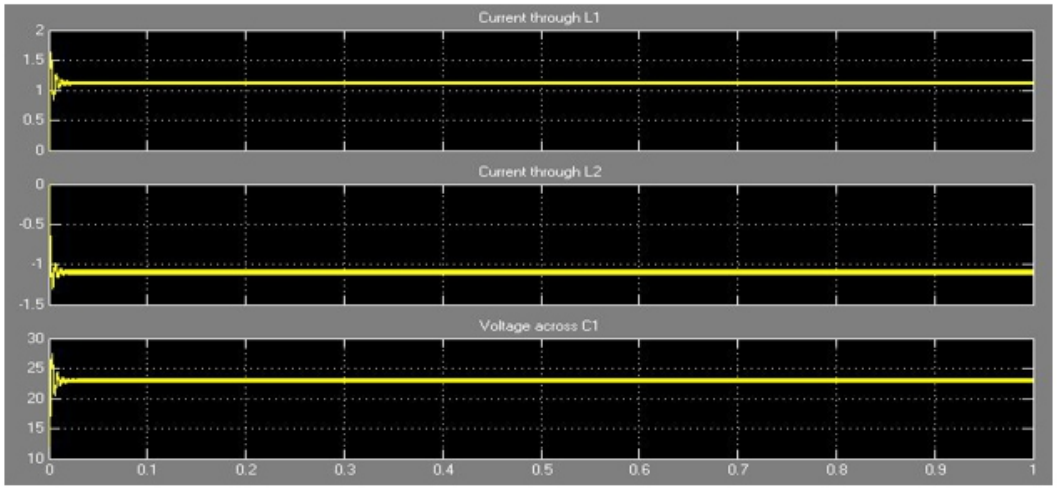

Fig 15: O/P of Cuk Converter 2 with 50% duty cycle

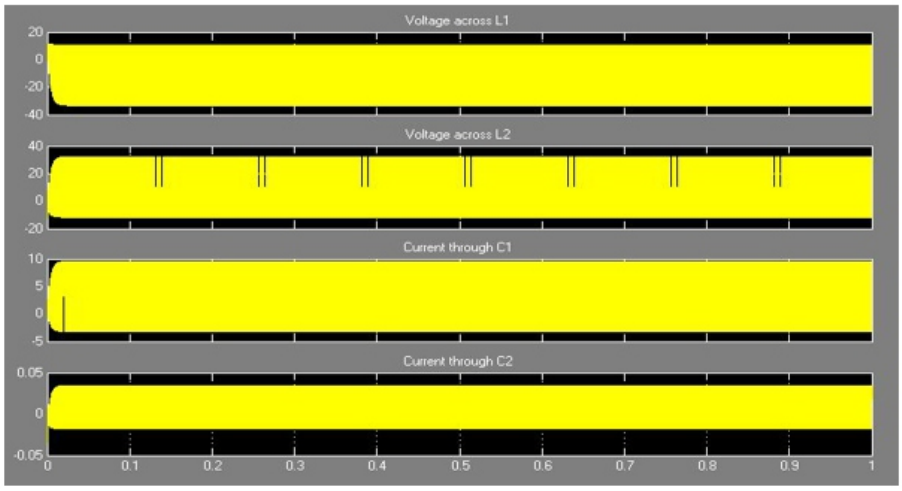

Fig 16 : O/P of Cuk Converter 1 with 75% duty cycle

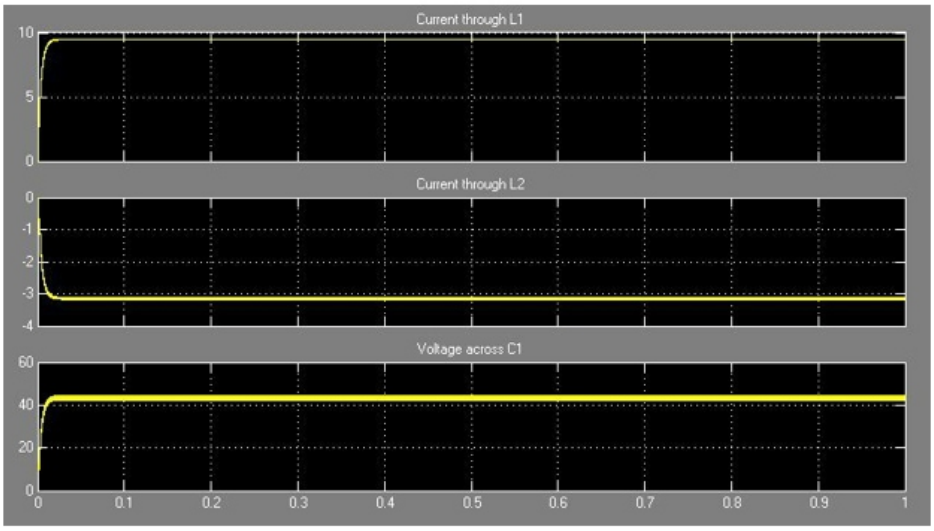

Fig 17: O/P of Cuk Converter 2 with 75% duty cycle O/P of PV System with MPPT

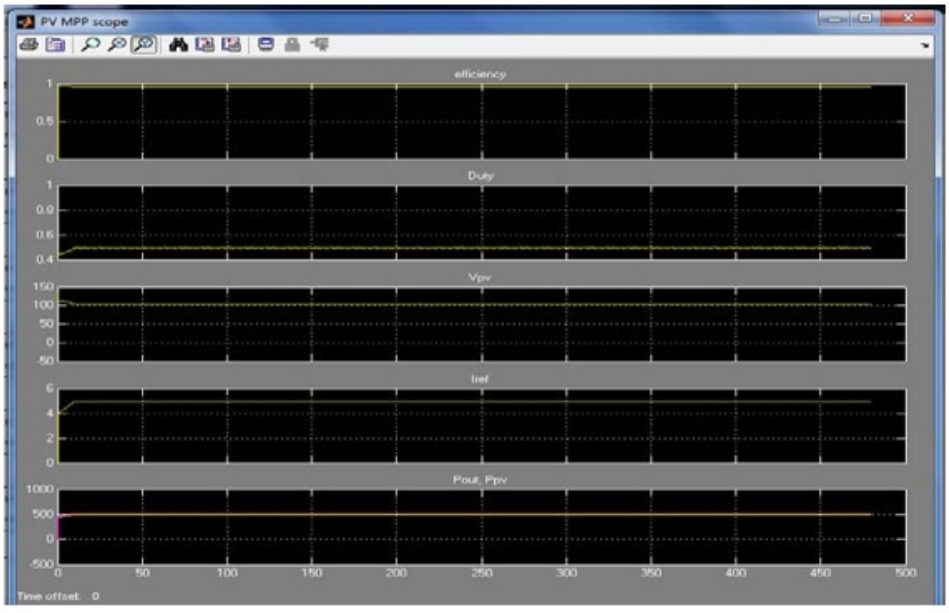

Fig 18: O/P of PV System

VI. CONCLUSION

Fig 18: O/P of PV System

With a well-designed system including a proper converter and selecting an efficient and proven algorithm, the implementation of MPPT is simple and can be easily constructed to achieve an acceptable efficiency level of the PV modules. From the comparison of 3 most popular MPPT technique - Incremental Conductance best MPPT technique. The outputs obtained from Incremental Conductance method were found to eliminate the limitations of Perturb & Observe Method. Cuk converter has many advantages as compared to other converter. It is found that at 50% duty cycle, the performance of convertor is better than other values of duty cycle. At this duty cycle, the input power is nearly equal to output power of Cuk converter. The proposed method offers different advantages which are: good tracking efficiency, response is high and well control for the extracted power.

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