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The International Journal of Microcircuits And Electronic

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Contents

Low Power High Speed Low Offset Regenerative Comparator

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ABSTRACT

In high speed ADC, a comparator directly influence the overall performance of ADC. In his paper we are reviewing different techniques for designing of comparators used in analog-to-digital converters. Following is a review for different techniques of low offset, high speed and regenerative type of preamplifier and latch structure. Two stages (preamplifier and latch) of comparator is provide a high speed which can then be implemented for low offset , high gain ,low threshold and low power. This implementation gives a high performance of a comparator. We are presenting details analysis of different techniques in this.

Index Terms: - Analog-to-Digital Converter, comparator, Digital logic, CMOS, latch.

Introduction

Comparators are fundamental building block for Analog-to-Digital converters and regulators. ADC's are used in many applications such as data storage systems, fast serial links, high speed communication and interfaces, which required for high resolution and high speed of the order of GSPS. In many applications comparator is a key element for conversion therefore widely used in circuit design. Basically it compares two analog inputs and gives a logical value at the output which depends on polarity of the input voltage different. Power consumption and speed are very important factors in comparator design. Low power consumption is very demanding for today's technology because it increases the battery lifetime. There have been many researches focusing on lowering the power consumption and using different techniques.

Architecture of a high speed comparator essentially consists of a preamplifier stage and alatching stage. In the pre-amplification stage the difference between the input signals is amplified thus the output voltage difference tracks the input signal. In the latching stage the output of amplification go through a digital logic level. This high speed comparator is further modified for increasing the performance of comparator.

This paper introduces a number of comparator design techniques for the use of ADC's. The techniques

II. Different Technique For Comparator Designing

There has been a growing demand for the development of low power circuit. Thus many researchers are trying to reduce the power consumption of any circuit. In this paper some different techniques are describing for low power comparators.

A. A Regenerative Comparator Structure With Integrated Inductors

A regenerative comparator structure with integrated inductors uses an inductor for improving the power consumption and sampling speed of comparator. Power consumption and sampling speed are two most important factors for comparator design. Sampling speed and power consumption of comparators improves as the transistor gate length is increased. Mostly comparators having two components: first a preamplifier and second a regenerative latch. Figure 1 shows the basic block diagram of comparator in which the combination of a transconductance and a load resistance represents a pre-amplifier and the combination of negative resistance and a load resistance represents a latch.

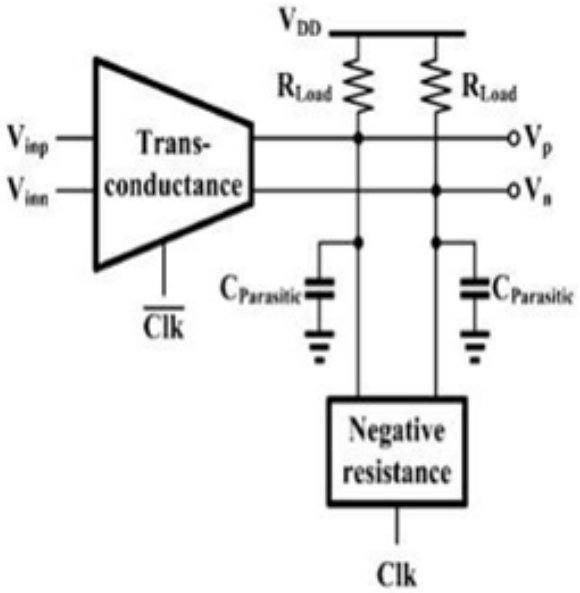

Figure 1

The operation of the comparator is controlled by the complementary clocks Clk and Clk'. When Clk is low, the comparator is in tracking mode and in this mode the latch is disabled, and the transconductance of preamplifier is enabled. The difference between input signals is amplified thus output voltage difference tracks the input signals. When Clk goes high latch is enabled and due to a negative resistance a regenerative circuit is formed which amplifies Vp and Vn to a digital logic level.

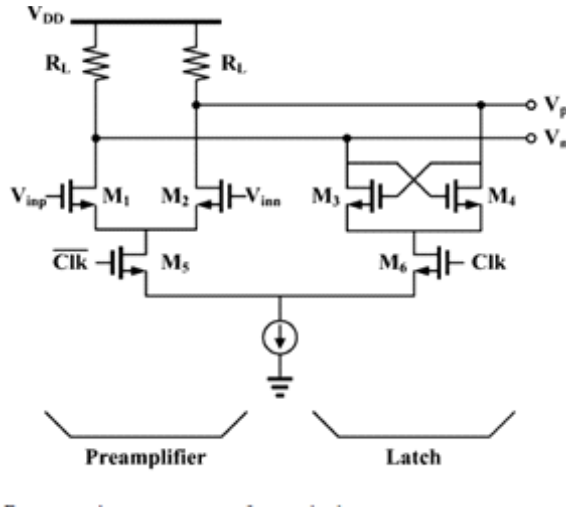

Figure 2

Figure 2 shows the circuit diagram for a regenerative comparator in which transistor M1-2 provide the transconductance for preamplifier and transistor M3-4 as cross coupled generate negative resistance for the latch. In the pre-amplification kick back noise reduces and also the offset of the latch reduces by the gain of the amplifier.

Implementation in Comparator Structure:

By the addition of inductor bandwidth in the pre-amplification stage is increased and the regenerative time constant decreased thus with the help of inductor both the tracking and latching speed is increased. The probability decreases exponentially with reduction in the regenerative time constant. Inductor is added to improve the performance of comparator. The inductor is connected in series with the load resistor. A large inductor parasitic is managed if the parasitic resistance is considered as a part of load resistor. The use of thinner metal lines in the inductor is beneficial for comparator.

B. A Novel 1gsps Low Offset Comparator For High Speed ADC

This paper describes a low power and ultra high speed low offset preamplifier-latch comparator. There have many types of comparators which provide high speed but the speed more than 1GSPS is hardly achieved because of the limitation of the bandwidth of amplifier. The dynamic latch comparator is used for high speed. In this comparator two negative resistances in parallel to load resistance are used. The comparator uses novel method to reduce the recovery time. This paper based on the analysis of the speed and offset of preamplifier-latch comparator.

Basic Operation:

The proposed comparator of this paper consists of a preamplifier, regenerative latch and output latch.

The input signals delivered to preamplifier which reduces the offset voltage. The regenerative latch compares the inputs and the output latch integrates the final output. The Clk signal is used in the regenerative mode to reduce the power consumption caused by the dynamic current of the transistor. The final output is generated by the the output latch.

Effected Parameters:

In high speed comparators at the preamplifiers stage the bandwidth is high thus the gain is also high to amplify the input signals. The proposed comparator the offset is caused by the preamplifier thus the offset voltage is reduced. The propagation delay of this paper is also reduces due to the channel length. Thus these parameters are changed for improved performance of the comparator.

C. A 0.35MM Cmos Comparator Circuit For High-speed Adc Applications

This paper presents a high speed differential clocked comparator circuit. The comparator circuit consists of a pre-amplifier and a latch stage with the dynamic latch at the output. At the output the circuit consists of a full transmission gate (TG) and two inverters which help in the reduction of power consumption.

Basic Blocks Diagram of Proposed Comparator:

The block diagram of the comparator is shown in figure 3 which consists of three main blocks a pre-amplifier, a latch and an output sampler. Transmission gate and inverter is used in output sampler and the combination of both acts as a holding capacitor. The outputs are sampled at the end of evaluation phase. The samples are amplified using the output inverters.

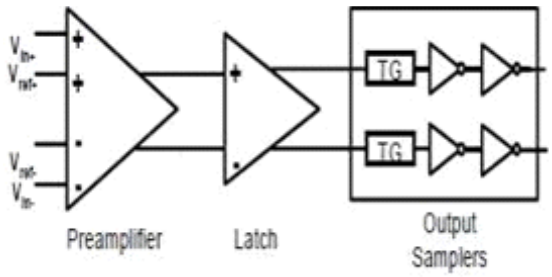

Figure 3

Implementation due to Transmission Gate

When a TG is used as a sampling switch, charge injection is occurs which creates some problems with the operation of the circuit. However in the proposed comparator architecture, voltage changes due to the charge injection and adds to the sampled signals.

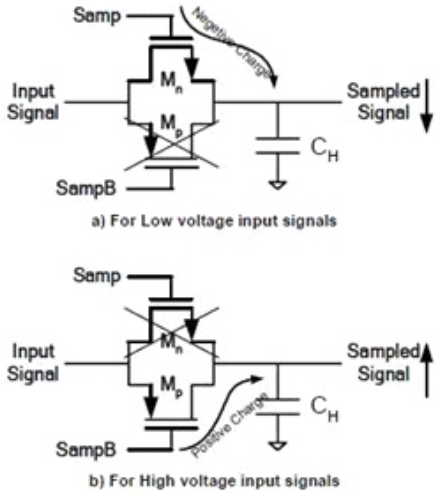

Figure 4

Figure 4 shows the effect of charge injection in TG, when TG is in track mode, "samp" is high and Mn transistor acts as closed switch for low input voltages. At the end of track mode "samp" changes to low and the Mn switch is opened. Thus the charge injection changes the voltage level.

III. Conclusion

There are different techniques are used for improving the performance of a comparator. By the addition of an inductor the load resistance is decreases thus the latching speed is increased. The technique become more beneficial with the smaller inductance as the gate length shrink. This technique is applicable to all type of comparators. In the novel method for high speed the comparator uses two negative resistors parallel with positive resistors as the load resistors of preamplifier to improve its gain thus the offset voltage is reduced. It is suitable for 1GSPS high speed ADC. By using a TG at the output sampler stage the power consumption of comparator is reduces. Also TG's charge injection enhances the voltage level of sampled signals.

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Analytical Study Of Analog Phase-locked Loop In Message Signals Transmission

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ABSTRACT

A phase-locked loop is a criticism framework consolidating a voltage controlled oscillator and a phase comparator so associated that the oscillator frequency (or phase) precisely tracks that of an connected frequency-or phase-tweaked signal. Phase-locked loops can be utilized, for instance, to produce stable yield frequency signals from a settled low-frequency signal. The first phase-locked loops were executed in the mid 1930s by a French architect, de Bellescize. In any case, they just discovered expansive acknowledgment in the commercial center when coordinated PLLs progressed toward becoming accessible as generally minimal effort components in the mid-1960s. The phase locked loop can be dissected as rules as a negative criticism framework with a forward pick up term and an input term.

Introduction

A modern propel technology in coordinated circuit technology makes fabrication processes exceptionally appropriate for digital outlines. Little territory and low-voltage plans are ordered by showcase prerequisites. Another favorable position of digital PLL is anything but difficult to update with the procedure changes. Since simple blocks are available in various digital and blended signal ICs, their overhaul is a vital factor in the arrival of another item. Nonetheless, the execution prerequisites of simple blocks requires a total upgrade in another procedure, along these lines expanding the outline process duration.

Decreasing the measure of simple circuitry can enhance the update of these blended signal ICs. A Phase Locked Loop is predominantly utilized with the end goal of synchronization of the frequency and phase of a privately created signal with that of an approaching signal. There are three components in a PLL. The Phase Frequency finder (PFD), the loop channel and the Voltage Controlled Oscillator (VCO). The VCO is the core of any PLL. The component by which this VCO works chooses the kind of the PLL circuit being utilized. There are essentially four sorts of constructing PLLs to be specific Direct PLL (LPLL), Digital PLL (DPLL) and All Digital PLL (ADPLL) [1].

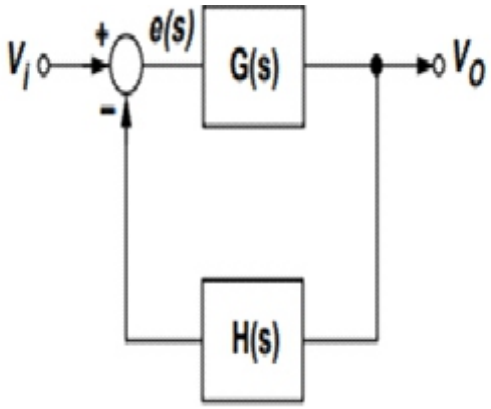

Figure 1. Standard negative-feedback control system model.

In a phase-locked loop, the error signal from the phase comparator is the contrast between the information frequency or phase and that of the signal input. The framework will compel the frequency or phase error signal to zero in the relentless state. The regular conditions for a negative-feedback framework apply.

Forward Gain = G(s), *s = jω = j2πf+
Loop Gain = G(s) × H(s)
Closed Loop Gain G s GsHs − = + ( ) 1 () ()

Because of the integration in the loop, at low frequencies the steady state gain, G(s), is high and VO/VI, Closed-Loop Gain = 1 H

The components of a PLL that contribute to the loop gain include:

1. The phase detector (PD) and charge pump (CP).
2. The loop filter, with a transfer function of Z(s)
3. The voltage-controlled oscillator (VCO), with a sensitivity of KV/s
4. The feedback divider, 1/N

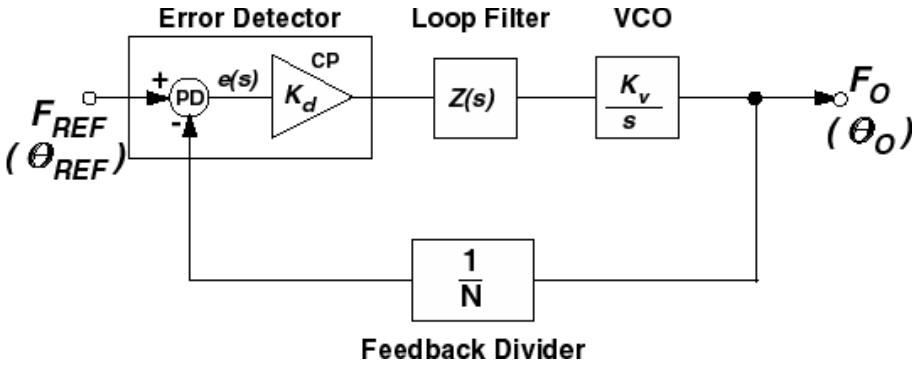

Figure 2.Basic phase-locked-loop model.

In the event that a linear component like a four-quadrant multiplier is utilized as the phase detector, and the loop channel and VCO are additionally simple elements, this is called a simple, or linear PLL (LPLL). In the event that a digital phase detector (EXOR door or J-K flip flounder) is utilized, and everything else remains the same, the framework is known as a digital PLL (DPLL).

In the event that the PLL is fabricated only from digital blocks, with no inactive components or linear elements, it turns into an all-digital PLL (ADPLL) [2].

Finally, with data in digital frame, and the accessibility of adequately quick handling, it is likewise conceivable to create PLLs in the product space. The PLL work is performed by programming and keeps running on a DSP. This is known as a product PLL (SPLL). Alluding to Figure 2, a framework for utilizing a PLL to produce higher frequencies than the info, the VCO sways at an precise frequency of ωD. A bit of this frequency/phase signal is nourished back to the error detector, by means of a frequency divider with a proportion 1/N. This isolated down frequency is nourished to one contribution of the error detector. The other contribution to this illustration is a settled reference frequency/phase. The error detector thinks about the signals at the two sources of info. At the point when the two signal information sources are equivalent in phase and frequency, the error will be zero and the loop is said to be in a "locked" condition. In the event that we essentially take a gander at the error signal, the accompanying equations might be developed [3].

$$e\,s = F_{REF} - \frac{F_0}{N}$$

When

$$e\,s = 0, \quad \frac{0}{N} = F_{REF}$$

Thus

$$F_0 = N\,F_{REF}$$

In business PLLs, the phase detector and charge pump together shape the error detector square. At the point when FO ≠ N FREF, the error detector will yield source/sink current heartbeats to the low pass loop channel. This smoothes the present heartbeats into a voltage which thus drives the VCO. The VCO frequency will at that point increment or lessening as fundamental, by KV ΔV, where KV is the VCO affectability in MHz/Volt and ΔV is the change in VCO input voltage. This will proceed until e(s) is zero and the loop is locked. The charge pump and VCO therefore fills in as an integrator, trying to increment or diminishing its yield frequency to the esteem required in order to reestablish its contribution (from the phase detector) to zero.

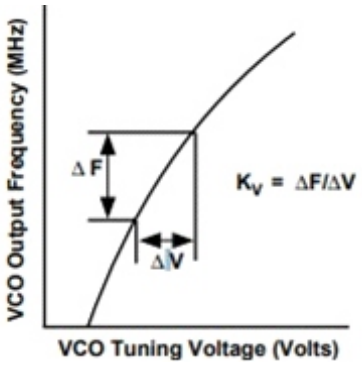

Figure 3. VCO transfer function

The overall transfer function (CLG or Closed-Loop Gain) of the PLL can be expressed simply by using the CLG expression for a negative feedback system as given above.

$$\frac{F_0}{F_{REF}} = \frac{Forward\ Gain}{1 + Loop\ Gain}$$

$$Forward\ Gain, G = \frac{K_D K_V Z(s)}{s}$$

$$Loop\ Gain, GH = \frac{K_D K_V Z(s)}{N_s}$$

When GH is much greater than 1, we can say that the closed loop transfer function for the PLL system is N and so

$$F_{OUT} = N \times F_{Ref}$$

2. PLL Applications To Frequency Upscaling

The phase-locked loop enables stable high frequencies to be produced from a low-frequency reference. Any framework that requires stable high frequency tuning can profit by the PLL method. Cases of these applications incorporate remote base stations, remote handsets, pagers, CATV frameworks, clock recovery and - era frameworks. A decent case of a PLL application is a GSM handset or base station. Figure 4 demonstrates the get segment of a GSM base station. In the GSM framework, there are 124 channels (8 clients for each channel) of 200-kHz width in the RF band. The aggregate bandwidth involved is 24.8 MHz, which must be examined for action. The handset has a transmit (Tx) scope of 880 MHz to 915 MHz and a get (Rx) scope of 925 MHz to 960 MHz. On the other hand, the base station has a Tx scope of 925 MHz to 960 MHz and a Rx extend of 880 MHz to 915 MHz. For this illustration, we will consider just the base station transmit and get areas. The frequency bands for GSM900 and DCS1800 Base Station Systems are appeared in Table 1. Table 2 demonstrates the channel numbers for the transporter frequencies (RF channels) inside the frequency bands of Table 1. Fl(n) is the inside frequency of the RF direct in the bring down band (Rx) and Fu(n) is the relating frequency in the upper band (Tx)

Table 1.1: Frequency Bands for GSM900 and Base Station Systems

	T_x	R_x
P-GSM900	935 to 960 MHz	890 to 915 MHz
DCS1800	1805 to 1880 MHz	1710 to 1785 MHz
E-GSM900	925 to 960 MHz	880 to 915 MHz

3. Literature Review

The English physicist Edward Appleton initially portrayed the PLL and it showed up in the Proceedings of the Cambridge Philosophical Society in 1923.In 1953, Gruen distributed a paper particularly on the subject of automatic recurrence control use of PLL in shading TV transmission and gathering. In the year 1979, Gardner, F. examined insights about of PLL. He examined about fundamental standards of phase lock operation, ordinary practices of phase lock building and utilizations of phase lock to different issues. A compact audit of the fundamental PLL standards material to correspondence and control frameworks was displayed by Hsieh, G.C. and, Hung, J.C. in the year 1996.

4. Objectives

The primary target of the proposed work is to display and mimic a moment arrange APLL in time space to ponder the accompanying:

1. To study the transient behavior of phase-locked loop in analog communication
2. To study the Analog Phase Locked Loop in time domain model
3. To study the multiplexing model and its techniques in analog communication
4. To study the dynamic parameters in multiplexing and phase-locked loop in analog communication

5. Research Methodology

The simulations are conveyed outing Turbo C and MATLAB stage. Turbo C is a compiler for C programming dialect from Borland. It was first presented in 1987 and it is noted for its coordinated improvement environment, little size and quick ordering speed. With Turbo C, there is no requirement for a different proofreader, compiler and linker to run the C programs. The primary focal points of C codes are the enhanced precision and adaptability as nonlinear algebraic and differential conditions can be proficiently spoken to. The simulation speed can be essentially expanded by utilizing pre-assembled

computer languages, for example, C. As C programming permits abnormal state displaying of useful pieces, along these lines, it is greatly useful for the framework level outline and optimization of framework parameters.

The methodology towards implementation of the proposed work for achieving the objectives as:

1. Derivation of a theoretical model for second order APLL considering different block of elements.
2. Derivation of a theoretical model for circuit level simulation of the LF.
3. Derivation of companion network model for non linear element of the LF based on Backward Euler numeric integration method.
4. Derivation of mathematical model for VCO and multiplier type PD of the model.
5. Derivation of a model for phase error process to study the cycle slips behavior of the model.
6. Derivation of an AWGN model for the APLL.
7. Derivation of a generalized model for the APLL considering different blocks.
8. Simulation of the APLL model by using Turbo C program to study the dynamic characteristics of the PLL and effects of noise on the system.

We are using following tools & methods in our research work:

- Design of an algorithm for the proposed APLL model for simulation in time domain using the Gauss-Seidel iterative method.

The Gauss-Seidel algorithm

1. Take the necessary vectors and arrays as inputs
2. Select an initial guess to start the iteration
3. Solve. Using the Gauss-Seidel Method
4. Check convergence conditions
5. IfConvergence is satisfied go to step

- Developing the simulation program incorporating iterative solution options for adjustment of convergence condition, Tsim, T, absolute relative error and tolerance value.
- Developing the simulation program for studying the effects of noise on APLL dynamics.
- Developing the simulation program to study the RMS, histogram and PE) F of phase error behavior.
- Simulating the model to plot the time-domain voltage waveforms of the APLL model.
- Simulating the model to extract the phase and frequency information from time-domain voltage waveforms of the model. The next chapter of the thesis will present in details the theoretical estimation for the proposed APLL model.

6. Results

Phase frequency detector and DCO reproductions are finished utilizing Xilinx and reenactment waveform of same is appeared beneath. The outline has been finished remembering the versatility, adaptability and optimal standard. It can be utilized as a part of any outline suiting the given frequency determinations. A framework clock of 5 MHz is utilized. The plan is executed for a middle frequency of 300 kHz. It's chiefly implied for low frequency applications. The present outline offers a working frequency scope of 290 kHz to 320 kHz around. The outline can be stretched out past that too. Be that as it may, the rationale model should be changed to overcome the proliferation defer that is acquainted due with more noteworthy number of bits engaged with the calculation.

7. Conclusion

As indicated by audit of ADPLL, digital circuits are more adaptable, proficient, adaptable, and less loud as contrasted with simple circuit. This paper talks about the ADPLL configuration utilizing Verilog HDL It likewise displays the FPGA execution in detail. The ADPLL blocks utilized for the outline are additionally given here. This PLL is intended for the middle frequency of 200 kHz and its working frequency scope of ADPLL is 189 kHz to 215 kHz, which is the bolt scope of the plan. At the point when the info was to blame, it consequently continued output arrangement by utilizing the last known right parameters.

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An Disseminate System To Control And Communicate UGV And MAV

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ABSTRACT

This paper represents a communication and control systems based surveillance for Unmanned Ground Vehicle (UGV) – Micro Air Vehicle (MAV). Radio Frequency (RF) relay based control and communication system is used to communicate between the vehicles and ground station. These control systems are meant to inscribe a large number of military and civilian applications counting reconnaissance, intelligence and surveillance in collusion with communication network. A First Person View (FPV) approach is employed to regulate the vehicles wirelessly. This paper discusses the on-board computation methodology of the vehicles and communication system with ground station through a custom interface. The integrated system concludes to present a technique to control and coordinate a robotic surveillance system.

Index Terms—*Micro Air Vehicle, Relay Communication, Surveillance, Unmanned Ground Vehicle.*

Introduction

Unmanned vehicles1 are meant to accomplish the affair of reconnaissance, intelligence and surveillance. The control and communication between ground station and these vehicles is accomplished using a regulating operation and custom interface. Without a human pilot on board an unmanned vehicle, like UGV2 and MAV3, are autonomous or wirelessly controlled vehicle, having motion controlled either autonomously by computers in the vehicle, or under the remote control of a pilot on the ground or in another vehicle. The presented system in this research, as shown in Fig. 1, consists of an Unmanned Ground Vehicle (UGV), a flapping type Micro Air Vehicle (MAV) and a Base Station with communication devices and laptops.

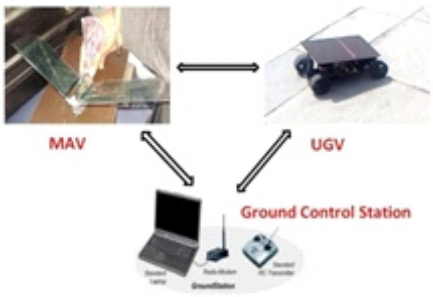

Fig.1. Developed system consisting of UGV-MAV-Ground Station

Unmanned system based surveillance entails long range data transmission and operation. The entire mission plan incorporates the execution of UGV as the launch vehicle for MAV and a relay with repeater on it. As RF modules issue an authentic method of communication, which is used between the above discussed systems. During the mission, the operation is to be performed for a range of 3 km and the wireless RF module available in India was not of craved range to control the MAV directly from base station. Accordingly, on the UGV a relay circuit subsisting of two RF modules was used. The task was accomplished by deploying the UGV up to the 500m range after which, the MAV was launched from it. In a system, these vehicles together extant various civilian and military applications in the field of surveillance and intelligence with a video camera and sensors equipped on both the vehicles.

II. Control And Coordination Structure Delineation

A. UGV Control System

The delineation of available UGV system was achieved by instrumenting the vehicle for computer controlled operation. The UGV consists of subsystems including drivetrain, 2- axis pan tilt system, on board camera, sensors and servo motors for navigation. The UGV has been developed to evolve relay system for communication and to take the MAV from Ground Control Station to the 500m mark. It is propelled by 5 Kg-Cm Torque DC Brushless motor, 1000 RPM and the rating of 12V and 2 Amps. To achieve UGV forward and backward motion the above mentioned high torque and high rpm motor. This motor is connected to the differential gear which propels the vehicle making it a 2 wheel drive. By using the steering system the direction control of the UGV is attained which is actuated by the Servo motor, providing precise steering, thus helping in maintaining the stability. These motors and servos is Arduino Mini Board consisting of Atmel's Atmega 328 microcontroller is controlled by the system hardware, which is considered to be compact, highly efficient and reliable. Fig. 2 shows the on-board circuit diagram of the UGV.

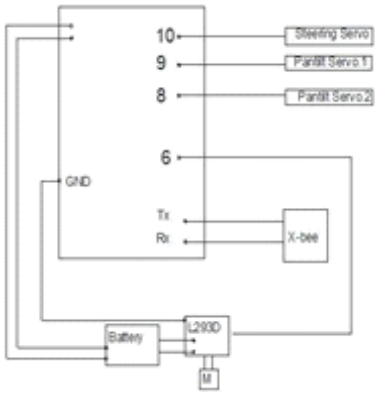

Fig.2.On-board circuit diagram-UGV

As shown in Fig. 2 circuit diagram, motor M the main drivetrain motor controlled by L293D controller. Also, the steering system drives by a servo motor and two servo motor combines to make a pan-tilt system, which are attached to the microcontroller. The programme code to control the vehicle wirelessly from base station is done using Arduino 1.0.5 Software as shown in Fig. 3 below.

Fig.3. Programming code in Arduino 1.0.5

```
*/
#include <Servo.h>

Servo myservo;
Servo myservo1;
Servo myservo2;
int motorPin = 6;
int m2 = 7;
int pos = 130;
int inByte = 0;

int pos1=100;
int pos2=100;
void setup()
{
 Serial.begin(9600);
 myservo.attach(9);
 myservo1.attach(10);
 myservo2.attach(11);
 myservo.write(130);
 myservo1.write(100);
```

```
Continue.....
void loop()
{

 digitalWrite(12,HIGH);
 if (Serial.available() > 0) {
 inByte = Serial.read();
 if (inByte=='q' &&
pos<=160){
 pos=pos + 10;
 myservo.write(pos);
 delay(05);
 }
 else if (inByte=='r' &&
pos> 100){
 pos=pos - 10;
 myservo.write(pos);
 delay(05);
 }
 else if (inByte=='o' &&
pos1> 60){
```

```
pos1=pos1 + 10;
myservo1.write(pos1);
delay(05);
}
else if (inByte=='u' &&
pos2> 60){

pos2=pos2 - 10;
myservo2.write(pos2);
delay(05);
}
else if (inByte=='i' &&
pos2<140){
 pos2=pos2 + 10;
 myservo2.write(pos2);
 delay(05);
 }
 else if (inByte=='z'){
 digitalWrite(motorPin,1);
 }
 else if (inByte=='c'){
```

Motor Type	Forward	Stop	Left	Right	Up	Down
Drive Motor M	Key Z	Key X	N/A	N/A	N/A	N/A
Steer Servo S	N/A	N/A	Key Q	Key R	N/A	N/A
Pan Servo P	N/A	N/A	Key O	Key P	N/A	N/A
Tilt Servo T	N/A	N/A	N/A	N/A	Key I	Key U

Software for UGV microcontroller To control the UGV system from base station, a custom interface of X-Bee transceiver with X-CTU software was defined with allotment of Keyboard keys for various functions as discussed in Table 1 below. The vehicle was controlled for forward motion and stop. The other servos involved in steering and pan-tilt is controlled for left-right and up-down motion.

Table1. UGV Motor control key allotment on base station keyboard

B. MAV Control System

The system design for proposed combination requires a robust methodology and flow to define the control and communication architecture. Inspirations were taken from birds which create lift by flapping its wing and navigate through its tail. System to control and communicate was developed with the efforts of mechatronics. The design of MAV resembles bottom-up approach enhanced with bio mimicry to develop a flapping wing MAV.

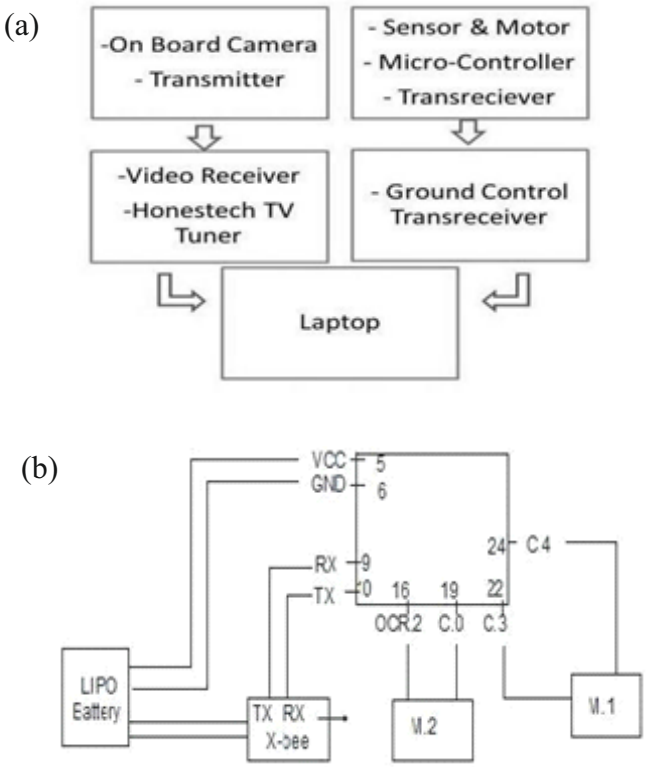

Fig.4. (a) Control loop diagram; (b) MAV on-board circuit diagram

The control loop diagram, as shown in Fig. 4(a), for both FPV system and control of MAV, starts with collecting all the sensor and video data which are streamed back to the ground control station from on-board computer. Control commands are sent back to the MAV by a custom interface after processing these data and the trainer function on X-bee transceiver which allows switching between human control and computer. As shown in Fig. 4(b) circuit diagram, the motor M1 drives the flapping mechanism and M2 controls the tail navigation. These motors are controlled using Atmel's Atmega 16L microprocessor for its inbuilt PWM ports and small size, resulting into elimination of motor controlling IC causing weight reduction of circuit board. The Micro-controller is interfaced to a 2.4GHz X-bee transceiver to provide data link with ground station at up to 250kbps data rate. Using BASCOM software, the

programmes need to be burnt for computation and functioning of microcontroller. Further this programming was burnt on the microcontroller with AVR Dude Software. The codes for the mentioned programmes are shown in Fig. 5 below.

```
$regfile = "m16def.dat"
$crystal = 2000000
$baud = 9600
Config Timer2 = Pwm,
Pwm = On, Prescale = 1,
Compare Pwm = Clear Up
Start Timer2
Config Portc.0 = Output
Config Portc.3 = Output
Config Portc.4 = Output
Dim A As String * 1
Do
Cls
A = Waitkey() Continue....
Continue.....
If A = "a" Then
Ocr2 = 255
Portc.0 = 0
Elseif A = "s" Then
Ocr2 = 200
Portc.0 = 0
Elseif A = "d" Then
Ocr2 = 130
Portc.0 = 0
Elseif A = "f" Then
Ocr2 = 70
Portc.0 = 0
Elseif A = "g" Then Cont...
Continue...Ocr2 = 0
Portc.0 = 0
Elseif A = "b" Then
Portc.3 = 1
Portc.4 = 0
Elseif A = "n" Then
Portc.3 = 0
Portc.4 = 0
Elseif A = "m" Then
Portc.3 = 0
Portc.4 = 1
End If
Loop
End
```

Fig.5. Programming code in AVR Dude

Motor Type	Maximum	Medium	Slow	Slowest	Stop	Clockwise	Anti-Clockwise
Drive Motor M1	Key A	Key S	Key D	Key F	Key G	N/A	N/A
Rear Motor M2	N/A	N/A	N/A	N/A	Key N	Key B	Key M

software for MAV microcontroller

Table2. Motor control key allotment on base station keyboard

To control the MAV motors from base station, a custom interface of X-Bee transceiver with X-CTU software was defined with allotment of Keyboard keys for various functions as discussed in Table 2 above. The speed of flapper was controlled in four steps as maximum, medium, slow and slowest. The rear motor involved for direction control was provided for clockwise and anticlockwise motion for left and right turn respectively.

C. FPV Data Transmission

As both UGV and MAV are piloted manually using FPV camera system, they are equipped with light weight camera system transmitting real time data to base station. Both the vehicles (UGV and MAV) are equipped with a 5.8 GHz wireless camera which has an about 3.5 km of range. This camera has an overall weight of 1 gm. and with video transmitter the total weight is 4 gm. It is also compatible with a

microphone which is placed for surveillance. Fig. 6(a) shows the on-board camera circuit on the vehicle and Fig 6(b) shows the receiver circuit at the base station.

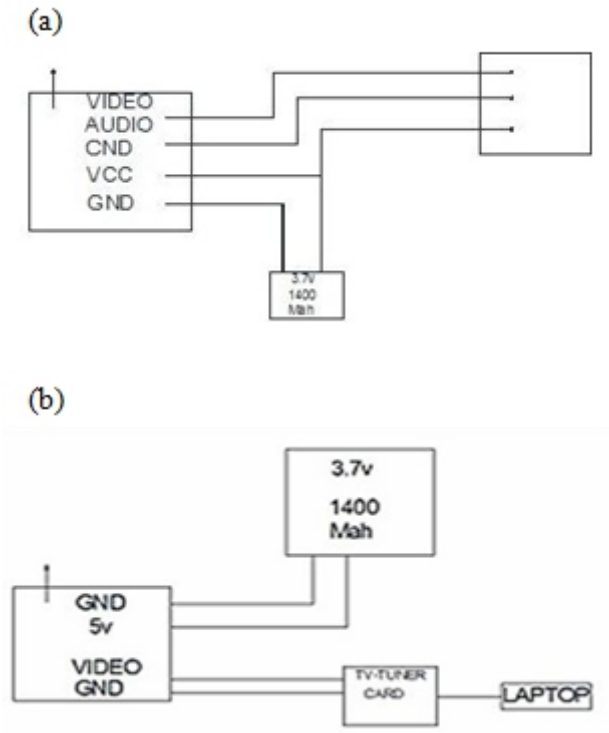

Fig.6. (a) On-board Camera circuit on vehicle; (b) Base station camera data receiver circuit

For electronic power sources LiPo batteries are used on the vehicles as they have a long life and better power to mass ratio. The pan-tilt system drives the UGV camera. TV Tuner card with Honestech TVR 2.5 Software is used on Ground Control Station, paired with laptop for receiving the video and Audio

D. MAV Relay Based Communication Channel

A relay system was implemented between UGV and MAV subsystem .As the mission to be accomplished using the developed system demands a range of 3 Km for MAV, with the implemented X-Bee system providing only 1.6 Km range. The X-Bee 2 and X-Bee 3, is made to act as a relay system providing a combined effect of 3.2 Km range of MAV. The relay system, as shown in Fig. 7 below, consists of a twin X-Bee transceiver on UGV.

To make it possible, as shown in the diagram, the transmitter pin of X-Bee 2 was joined with the receiver pin of X-Bee 3. The transceiver of 2.4GHz coupling created a relay system for MAV and PAN ID 23 was provided to the wireless module for functioning. When the MAV was in 1.6 Km range, the MAV is directly controlled by the base station, but when the MAV is out of 1.6 Km range, the relay system starts working on UGV and the coupled transceiver communicates with MAV. For this, the X-Bee 1 from

ground station gives command to X-Bee 2, which is approximately 1.6 km away from base station. Then the received data is communicated by X-Bee 3 to the MAV which is approximately again 1.6 Km from UGV and 3 Km from base station. Thus a 3.2 Km of range is acquired for surveillance using the developed system.

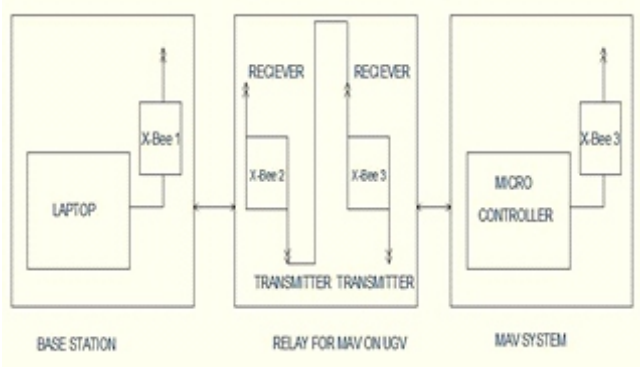

Fig.7. MAV System-Relay based communication channel

A robotic surveillance system based in FPV provides by the integrated approach of designing the control system for unmanned system and ground station together. The relay network as discussed above magnified the range of operation for the developed system.

III. Conclusion

With an overview of communication system architecture for an UGV-MAV based surveillance control system, (RF) radio frequency based data transmission methodology is discussed to perform various FPV based civilian and military operations. The use of microcontroller and its programming is an area of thirst for unmanned system development. Further, it is observed that the range of communication remains a major concern with these systems which can be tackled by designing relay network between multiple systems in a controlled and coordinated behavior. Thus it can be concluded that with recent advancement in on-board computation methodology among robotic surveillance system, a stable and secure communication channel can be demonstrated between ground control stations and unmanned systems.

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"Deployment Of Departmental Intercom Using IP Telephony"

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A B S T R A C T

The past decades we have witnessed a great progress towards applications of the wireless communication. It includes speech/ music transmission, computer related voice/music transmission. Wireless communication have been used in telephony such as cordless telephone, mobiles and Voice over IP (VoIP) is one of the most exciting new developments emerging within the telephony market. We are aware about the traditional PBX system. Traditional PBX systems can be replaced by IP PBX system in a cost effective way. Voice over IP (VoIP) has been implemented using different useful tools. One of the most efficient open source PBX systems is Asterisk PBX. Asterisk is released as open source under the GNU general public license (GPL) platform for IP PBX deployments. This paper provides architecture and deployment of IP PBX system using Asterisk.

Keywords: *wireless communication, VoIP, wireless LAN, PBX, IP phone.*

Introduction

Telephony history includes PSTN (public switch telephone network) which is based on circuit switching and data exchange network. It is very difficult to handle voice and data packets independently over the PSTN. The next trend developed in telephony to utilize all network resources is Voice over IP (VoIP) or IP telephony. It is used to transmit phone calls over the data network using Internet Protocol (IP). The term VoIP, not necessarily related to the internet; the protocol can be used on intranets and local area networks, in addition to both private and public wide area networks. IP-PBX is proposed system that includes the development of IP and soft switch which makes it possible to connect internet and telephone network.

2. IP-PBX System

Deployment of departmental intercom using IP telephony includes configuration of IP-PBX server which is considered as soft switch that uses packet switching technology. The second necessary requirement is one or more internet phones. Its working principle includes registering the clients i.e. soft phones to the server using shared wireless LAN. When client needs to call, it sends connection request to the server. Server has all SIP address of the users which is used to connect an internal call or external call using VoIP service

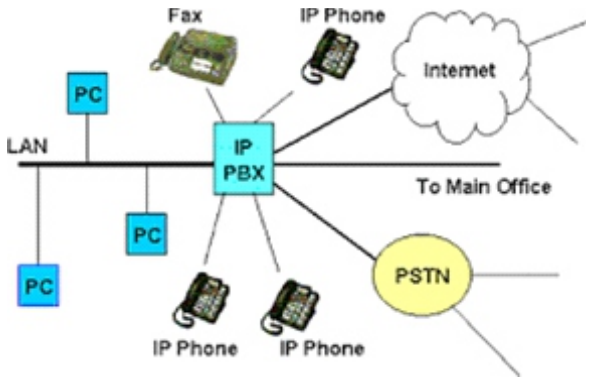

Figure 1: Architecture of IP PBX

Following are the advantages of IP-PBX over traditional PBX system.

- IP-PBX system is easy to install & configure as it is based on IP protocol.
- IP-PBX system provides significant cost savings using VoIP and Eliminate phone wiring in the case of addition of new phones in the network.
- Traditional PBX system requires external devices whereas the IP-PBX system is highly integrated.
- IP-PBX system is highly user friendly because of GUI compared to traditional PBX system.

3. Asterisk Platform

Now a day's most of the businesses are migrating to IP-PBX system instead of traditional PBX system because of low cost and high reliability. One of the most reliable IP-PBX is Asterisk Platform. Asterisk is released as open source under the GNU general public license (GPL) platform for IP PBX deployments. It provides all the features of the PBX using software and makes use of the LINUX environment. Commercial licensing is available from Linux Support Services, Inc. (http://www.linux-support.net) for applications in which the GPL is inappropriate.

Unlike many modern "soft switches", Asterisk can use both traditional TDM technology and packet voice (Voice over IP and Voice over Frame Relay) protocols. Calls switched on TDM interfaces provide lag-less TDM call quality, while retaining interoperability with VoIP packetized protocols.

To understand the basic difference between VoIP calls and ordinary phone calls, it is important to compare them with each other.

Packet Switching	Ordinary Telephony
• Standardized protocols and packet Formats • Very limited internal state • No session state in the network • Services can be added by anyone • No central control • Unclear what the role of operators is (or even who is an operator)	• Standardized interfaces • Lots of internal state (i.e., each switch & other network nodes) • Built in services by the network (hard to add new services) • Centralized control • Clear operator role

Table 1: Comparison between VoIP and Ordinary Telephony

The characteristics of Asterisk are [8],

- Supports for traditional analog telephony devices and digital telephone equipment.
- Supports for major VoIP protocols such as SIP, H.323, MGCP etc.
- Its own specific protocol IAX2 is used to communicate between the server and Asterisk.

3.1 Session Initiation Protocol (SIP)

Session Initiation Protocol is the IETF's standard for establishing VOIP connections. It is an application layer control protocol for creating, modifying and terminating sessions with one or more participants [18]. The architecture of SIP is similar to that of HTTP (client-server protocol). SIP has INVITE and ACK messages which define the process of opening a reliable channel over which call control messages may be passed. SIP makes minimal assumptions about the underlying transport protocol. This protocol itself provides reliability and does not depend on TCP for reliability. SIP depends on the Session Description Protocol (SDP) for carrying out the negotiation for codec identification. The services that SIP provides include [19].

- User Location: determination of the end system to be used for communication
- Call Setup: ringing and establishing call parameters at both called and calling party
- User Availability: determination of the willingness of the called party to engage in communications
- User Capabilities: determination of the media and media parameters to be used

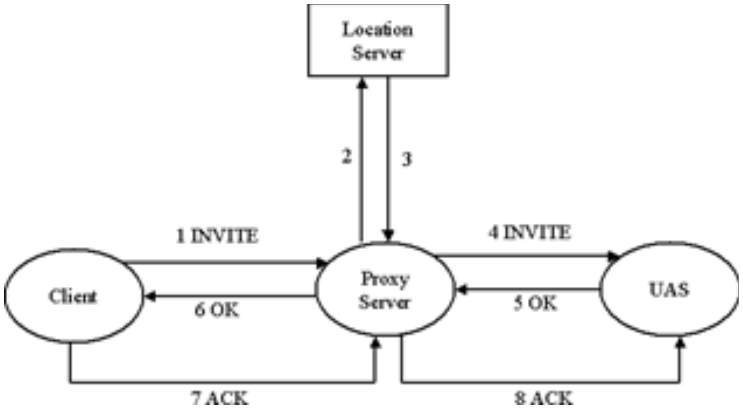

Figure 2: Sample SIP operation [19]

3.2 H.323 Standard

This is the ITU-T's (International Telecommunications Union) standard approved in 1996 used to promote Voice over IP service. H.323 is considered to be the standard for interoperability in audio, video and data transmissions, Internet phone and voice-over-IP (VoIP). It provides capability of addressing call control and management for both point-to-point and multipoint conferences as well as gateway administration of media traffic, bandwidth and user participation.

3.3 Media Gateway Control Protocol (MGCP)

MGCP is used for migration from PSTN to IP telephony, ISPs, and carriers by converting TDM circuits into voice packets. It is a protocol that defines communication between call control elements (Call Agents) and telephony gateways [2]. Protocol operates between a Media Gateway (MG) and a Media Gateway Controller (MGC), also known as Call Agents or Soft Switches, allowing the Media Gateway Controller to control the Media Gateway. MGCP is considered as part of the convergence movement that brings voice and data together on packet-switched Internet.

3.4 Supporting Protocols

SIP works in conjunction with RSVP (Resource Reservation Protocol), RTP/RTCP (Real-time Transport Protocol), RTSP (Real-time Streaming Protocol), SAP (Session Announcement Protocol) and SDP (Session Description Protocol). RTP/RTCP is used for transporting real time data, RSVP for reserving resources, RTSP for controlled delivery of streams, SAP for advertising multimedia sessions and SDP for describing multimedia sessions [19]. H.323. too works in conjunction with RTP and RTCP (Real-time Control Protocol). The present day voice gateways usually compose of two parts: the signaling gateway and the media gateway. The signaling gateway communicates with the media gateway using MGCP (Media Gateway Access Protocol). MGCP can interoperate with both SIP and

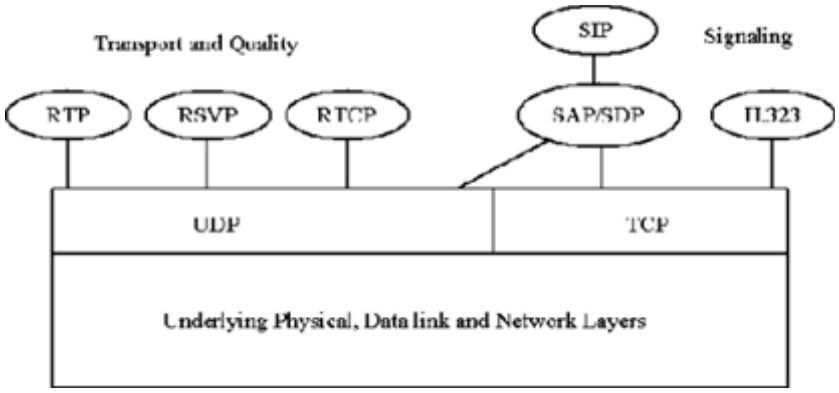

Figure 3: Supporting protocols for H.323 and SIP

4. Asterisk PBX Architecture

Asterisk architecture is fundamentally very simple and configured as the core of an IP or hybrid PBX, switching calls, managing routes, enabling features, and connecting callers with the outside world over IP, analog (POTS), and digital (T1/E1) connections. Asterisk runs on Linux, Mac OS X, Open BSD, FreeBSD and Sun Solaris and provides all features that are available in the traditional PBX system. Asterisk Telephony applications include features such as call bridging, conferencing, voicemail, auto attendant, custom IVR scripting, call parking, intercom and more. Asterisk has been carefully designed for maximum flexibility. Most of Asterisk's usefulness and flexibility come from the applications, codecs, channel drivers, file formats, and more, which plug into Asterisk's various programming interface [12].

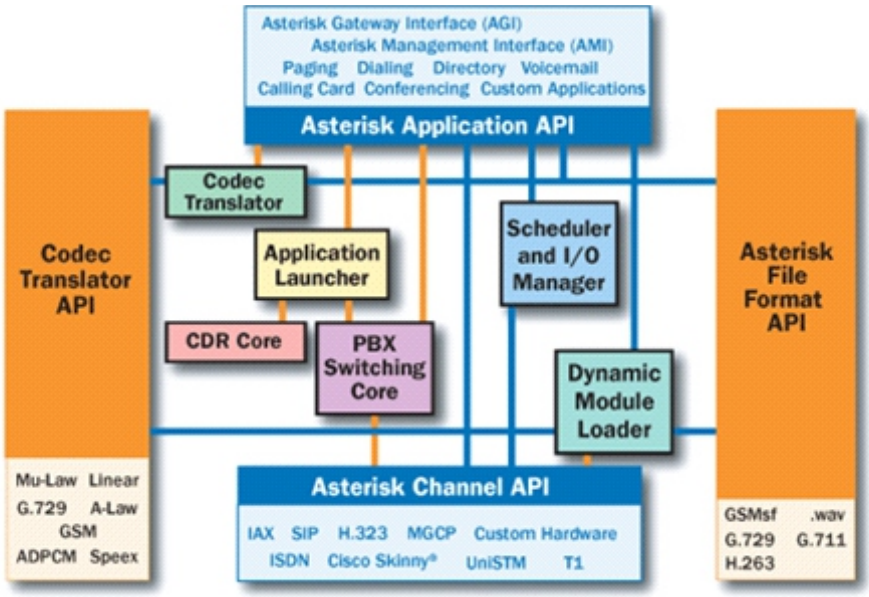

Figure 4: Architecture of Asterisk PBX

5. Experimental Results

In this section we present measurements of various parameters of proposed Voice over IP-PBX system. Voice over IP (VoIP) is susceptible to network behaviors, referred to as delay and jitter, which can degrade the voice application to the point of being unacceptable to the average user. Prior to deploying VoIP applications, it is important to assess the delay, jitter, and packet loss on the data network in order to determine if the voice applications work. The delay, jitter, and packet loss measurements can then aid in the correct design and configuration of traffic prioritization, as well as buffering parameters in the data network equipment.

5.1 The Goals of the Measurements

The goals of the measurements were four-fold:

- To gain understanding of the delay behavior of IP Voice;
- To measure the overall packet loss in VoIP links;
- To measure the total end-to-end delay (max. delta) including the processing delays at the workstations;
- To test the maximum inter-arrival jitter estimation of RTP in a new environment: IP Switching.

5.2 Choosing the Measurement Environments

In a VoIP PBX system, the main components are soft phones, Asterisk Call Manager and Wireless LAN. The Asterisk Call Manager software is the call-processing component of the Unified Communications system. It is an open source IP telephony call-processing solution. We are interested in IP voice delay, delay variance characteristics, maximum jitter and packet loss. These parameters are strongly affected by the type and amount of other traffic in the network. And hence we tried to put some load on our IP PBX server by originating more number of calls.

In this experiment, six IP PBX extensions (5000 to 5006) are created in the Asterisk server database that means six users are created in to the PBX system. A real-time VoIP traffic is generated by originating more number of VoIP calls using soft phone software named X Lite/CSipSimple. It is VoIP Telephony software which is not designed to simply duplicate the traditional telephone system. It is a suite of instant messaging and internet telephony software. PBX users can send and receive voice calls to or from other users on the Wireless LAN. In this test case, three calls are originated one after other.

A simple test bed was setup to transmit the voice packets through Asterisk Call Manager which is installed on Asterisk server computer connected to the Wireless LAN. One client is used to initiate calls and the other one receives calls on Wireless LAN with the help of soft phones.

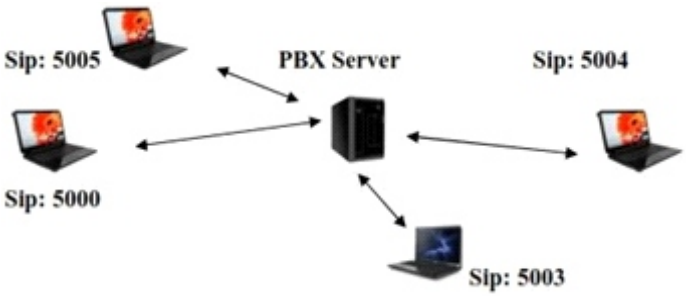

Figure 5: Measurement test bed setup

5.3 Data Capture and Analysis Tools

Wireshark is the primary protocol analysis software used to decode the trace file. From the decoded data, call setup processes and QoS parameters such as Maximum Delay, Maximum Jitter, Packet Loss and protocol mix of VoIP traffic can be determined. Wireshark is a popular network analyzer widely used by network professionals for troubleshooting, analysis, software and protocol development, and teaching. It reads packets from either the network or a trace file, decodes them, and presents them in an easy to understand format.

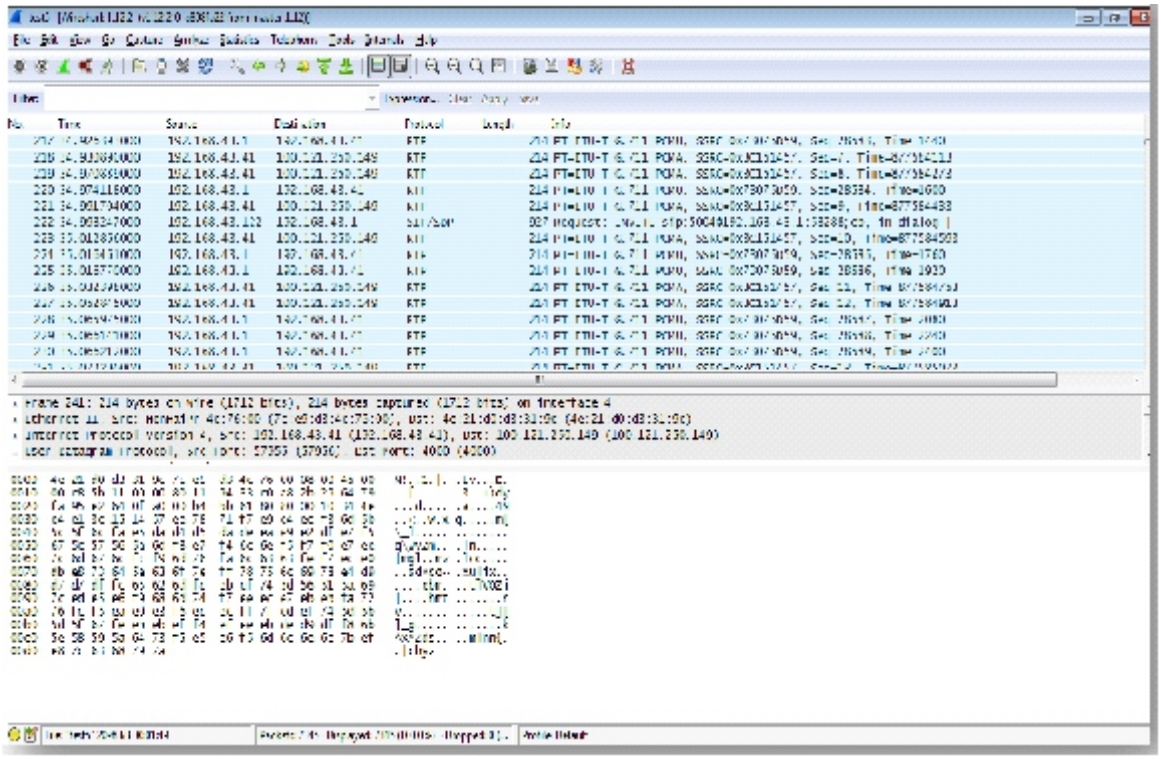

Figure 6: Wireshark captured file

Wireshark was chosen as the tool to use because it is an actively-maintained open source program and its graphical user interface is easily configurable and easy to use.

Following are the primary features to be utilized from Wireshark:

- It can capture data from the network or read from a captured file.

- It supports Tcpdump format capture filters.
- It runs on over 20 OS platforms, both UNIX-based and Windows.
- It supports over 480 protocols, and because it is open source, new ones are contributed very frequently.

5.4 Results: In this section, experimental results of test bed have been discussed along with the statistics are presented in detail.

5.5 Statistics

The information in the trace files of Wireshark is summarized in Table 2. In this experiment, a trace of three calls has been collected with approximately two minutes of voice data for each call. The traffic was captured from all the three bidirectional calls.

Attributes	Measured Values
Max. Delta	68.74 ms
Max. Jitter	13.23 ms
Lost RTP Packets	0 (0.00%)

Table 2: Overall statistics for the trace

Conclusion And Future Scope

The performance of IP PBX system is monitored on real-time basis and the performance (QoS) parameters are measured experimentally and are compared with the standard QoS parameters. Thus we can conclude that the measured values of QoS parameters are within the specified limits and hence proposed IP PBX system can be implemented in real-time environments. Lots of additional services can be implemented in the existing setup. These services may include interconnection with PSTN and Internet, advanced speech, web, and streaming video capabilities, Interactive Voice Response (IVR) services and many more. The total number of extension also can be increased with the help of dedicated PBX server.

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A New Symmetric Cascaded Multilevel Inverter Topology With Reduced Number Of Power Electronic Components

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ABSTRACT

Researchers try to improve the multilevel inverters performance or make them more economically proposing new switching algorithms or novel structures. In this paper, a new structure is proposed for symmetric cascaded multilevel inverter which has a simpler structure and uses fewer power switches compared to conventional cascaded inverter. The reduction in the number of power electronic devices will result in the reduction of the economic cost, installation area and switching losses. The proposed structure consists of a number of separate voltage sources at the input side to generate different voltage levels and an H-bridge at the output side. Switches also connect the input voltage sources to the output in a direct form or in series. Input sources can be isolated batteries or renewable energy sources such as solar cells and or fuel cells. Using fundamental switching frequency, the proposed inverter capable of generating 7 levels of voltage at the output, is simulated by use of MATLAB/SIMULINK software. The simulation results confirm the performance accuracy and capability of the proposed inverter to generate different voltage levels.

Keywords: *Multilevel inverter, Cascaded inverter, Symmetric structure, Asymmetric structure, H-bridge.*

Introduction

Voltage source inverters are categorized into two categories of two-level and multilevel inverters[1]. Multilevel inverters have many advantages over two-level inverters including: higher quality delivery power with lower harmonic at the output [2], use of components with lower voltage ratings, lower switching losses [3], higher efficiency, lower $\frac{dv}{dt}$ rate at the output and therefore lower stress on the load, higher voltage capacity and better electromagnetic compatibility [4]. Therefore, multilevel inverters have found many uses in industry including: use in micro-grids and distributed generation systems, renewable energy sources interface [5], static compensators [6], motor drivers [7], filters and FACTS devices [8]. Multilevel inverters are categorized into the three main categories of diode-clamped, flying capacitor and cascade[9-12]. Cascaded inverter, uses the lowest number of devices in its structure compared to the other two types [13]. Also, this inverter has higher voltage levels, power

(13.8kV & 30MVA) and reliability [14]. Given the ever increasing importance of multilevel inverters over recent years, different schemes have been developed to control these inverters, and the following ones are of special importance amongst these algorithms: sinusoidal pulse width modulation, pulse width modulation with selective harmonic elimination and space vector modulation [15].

II. Conventional Cascaded Inverter

This inverter is comprised of series connection of H-bridges. Each bridge consists of an input voltage source and 4 unidirectional switches with antiparallel diode and can generate three voltage levels of +VDC, 0 and –VDC at the output. The cascaded inverter is categorized into two categories of symmetric and asymmetric. The symmetric cascaded inverter uses input voltage source with equal values, and in this status, if n number of input voltage sources exist in each phase, then 2n+1 levels can be obtained in the output voltage [17]. In asymmetric cascaded inverter, input voltage sources have different values and can generate more voltage levels compared to symmetric cascaded inverter at the output. In this case, usually three incremental schemes called unary, binary and trinary are used to select input voltage sources values.

Figure 1. shows conventional cascaded inverter in the single phase form [16].

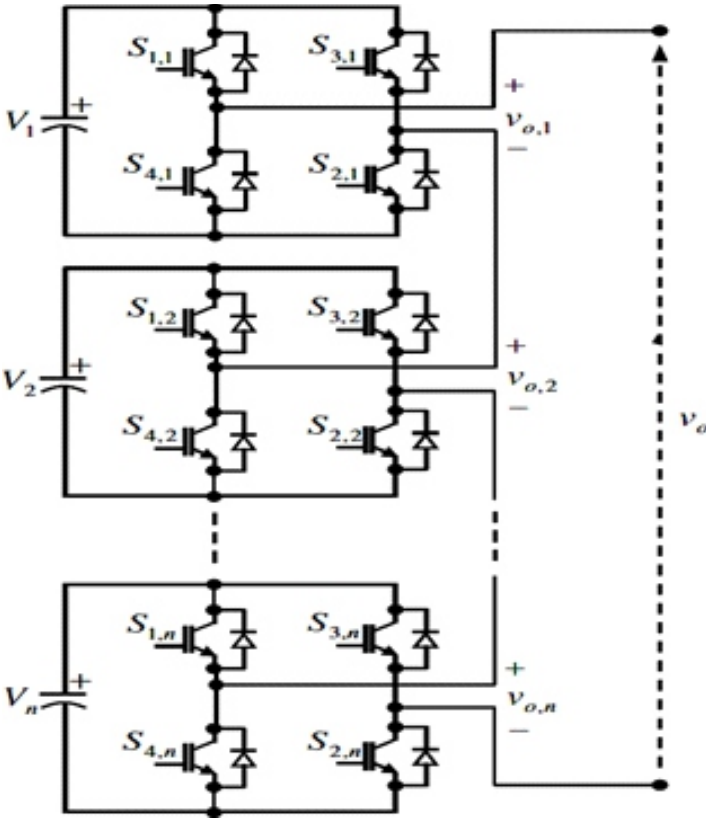

Figure 1. Conventional cascaded multilevel inverter topology in general

If n number of input voltage sources exist in the inverter structure, then Equation 1. shows the input sources values in the unary incremental scheme.

$$V_k = kV_1 \quad k = 2, 3, \ldots, n \qquad (1)$$

Equation 2. shows the input sources values in the binary incremental scheme.

$$V_{k+1} = 2^k V_1 \qquad k = 1, 2, 3, \ldots, n-1 \qquad (2)$$

Equation 3. shows the input sources values in the trinary incremental scheme.

$$V_{k+1} = 3^k V_1 \qquad k = 1, 2, 3, \ldots, n-1 \qquad (3)$$

Table 1. shows the number of generatable voltage levels at the output and also the number of switches for single phase conventional cascaded inverter in both symmetric and asymmetric modes.

Table 1. Conventional cascaded multilevel inverter number of switches and output voltages

		Asymmetric Mode		
	Symmetric Mode	Unary	Binary	Trinary
N_{level}	2n+1	n(n+1)+1	$2^{n+1}-1$	3^n
N_{switch}	4n	4n	4n	4n

III. The Proposed Topology

Figure 2. shows the proposed structure for symmetric cascaded inverter. As it is clear from the figure, this inverter consist of n voltage sources at the input side and 2n+2 number of switches. All circuit switches include a unidirectional IGBT with antiparallel diode. The polarity of input sources change alternatively and the H-bridge generates positive and negative voltage levels. Figure 3. shows a schematic comparison between the proposed inverter and conventional cascaded inverter in terms of the number of required power switches.

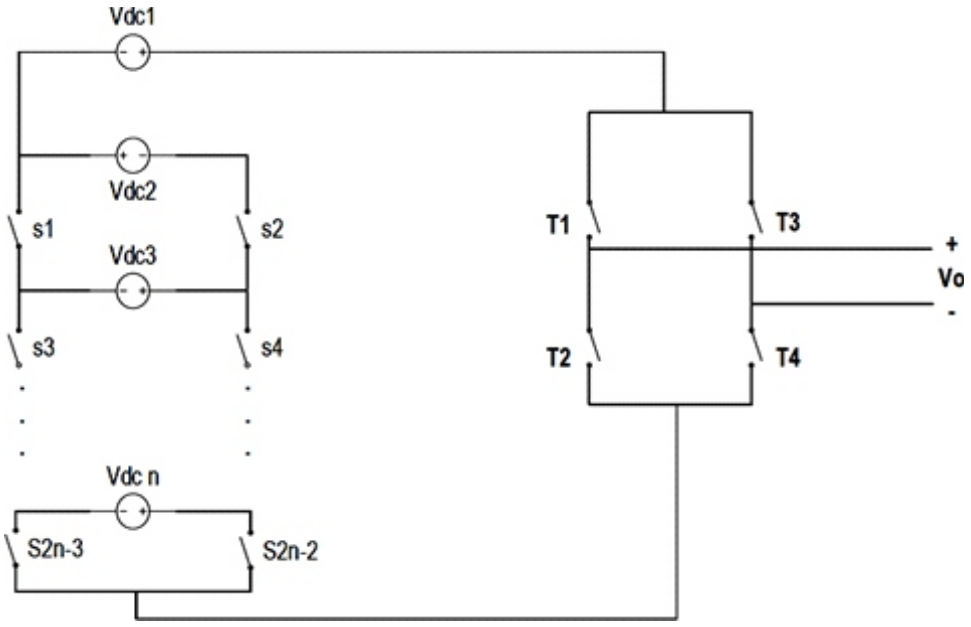

Figure 2. Proposed topology in general

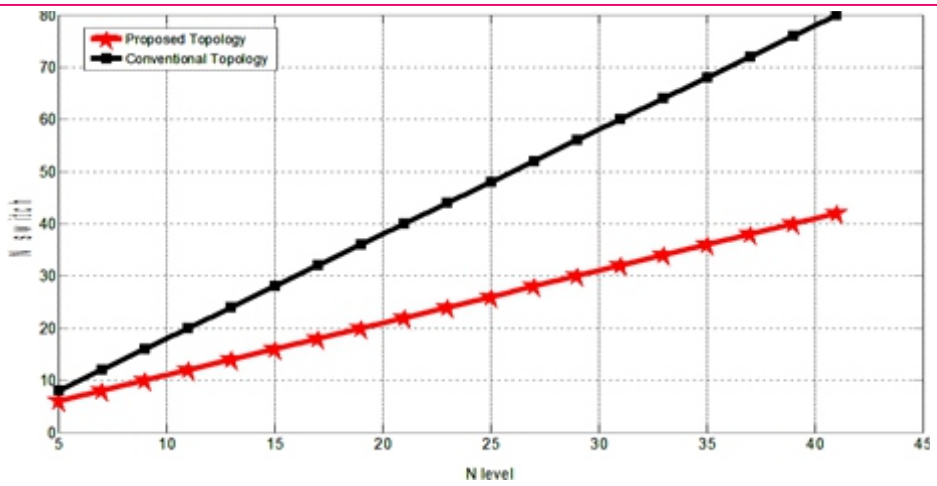

Figure 3. Comparison of the required number of switches to realize Nlevel voltage in conventional and proposed structures

Table 2. shows required switches and input voltage sources for some output voltage levels for proposed topology and conventional topology. According to Figure 3. and Table 2. the proposed inverter uses fewer switches compared to conventional cascaded inverter for the generation of different output voltages, which results in the reduction of the final cost of the inverter, installation area and switching losses.

Table 2. Required voltage sources and switches for proposed and conventional topology

Number of Input Sources	Number of Output Voltage Levels	Switches for Proposed Topology	Switches for Conventional Topology
3	7	8	12
5	11	12	20
7	15	16	28

IV. Case Study

Figure 4. shows the proposed inverter capable of generating 7 levels of output voltage. This inverter consists of 3 input voltage sources and 8 power switches. Table 3. shows the switching states and output voltage for this inverter. In this table, 1 means that the switch is ON and 0 means that the switch is OFF.

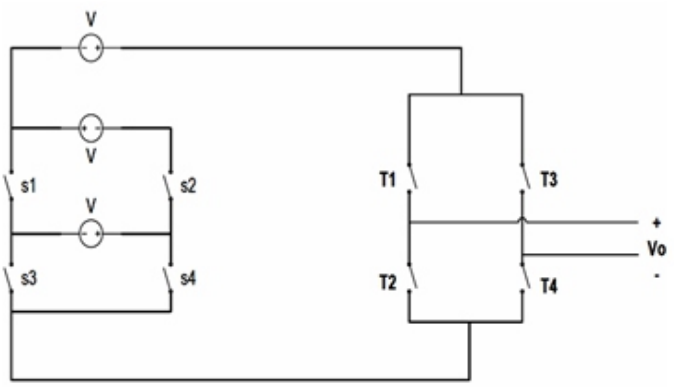

Figure 4. Proposed topology capable of generating 7 output voltage levels

Table 3. Switching states for 7 level proposed topology

S1	S2	S3	S4	T1	T2	T3	T4	Vo
0	0	0	0	1	0	1	0	**0**
1	0	1	0	1	0	0	1	**V**
0	1	0	1	1	0	0	1	**2V**
0	1	1	0	1	0	0	1	**3V**
1	0	1	0	0	1	1	0	**-V**
0	1	0	1	0	1	1	0	**-2V**
0	1	1	0	0	1	1	0	**-3V**

V. Simulation Results

In this section, we focus on the simulation of the inverter shown in the previous section with MATLAB/SIMULINK software. The voltage sources are considered with 200V and inductive ohmic load of L=400mH and R=15Ω. Figure 5. shows 7 levels output voltage and Figure 6. shows the harmonic spectrum of the output voltage. Figure 7. shows the load current and Figure 8. shows the harmonic spectrum and load current THD. As it is clear from Figure 7. the load current is approximately sinusoidal which represents the performance accuracy of the proposed inverter.

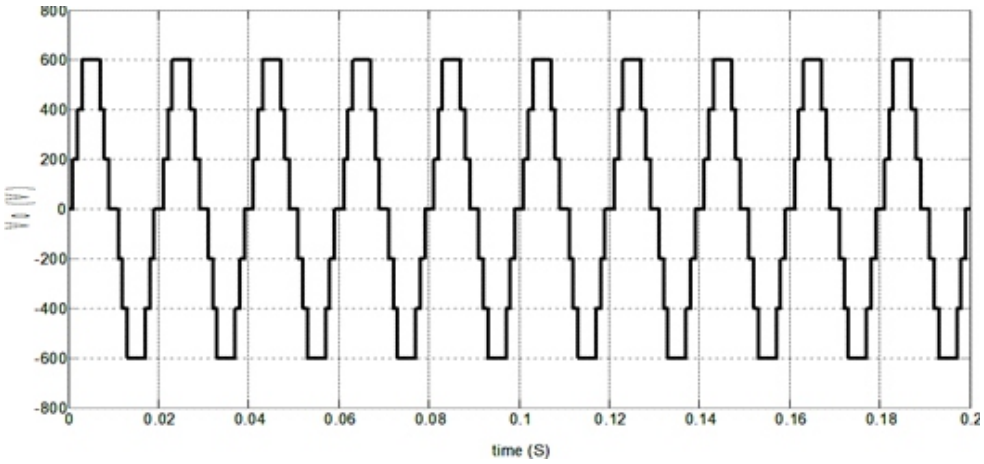

Figure 5. Output voltage with 7 levels

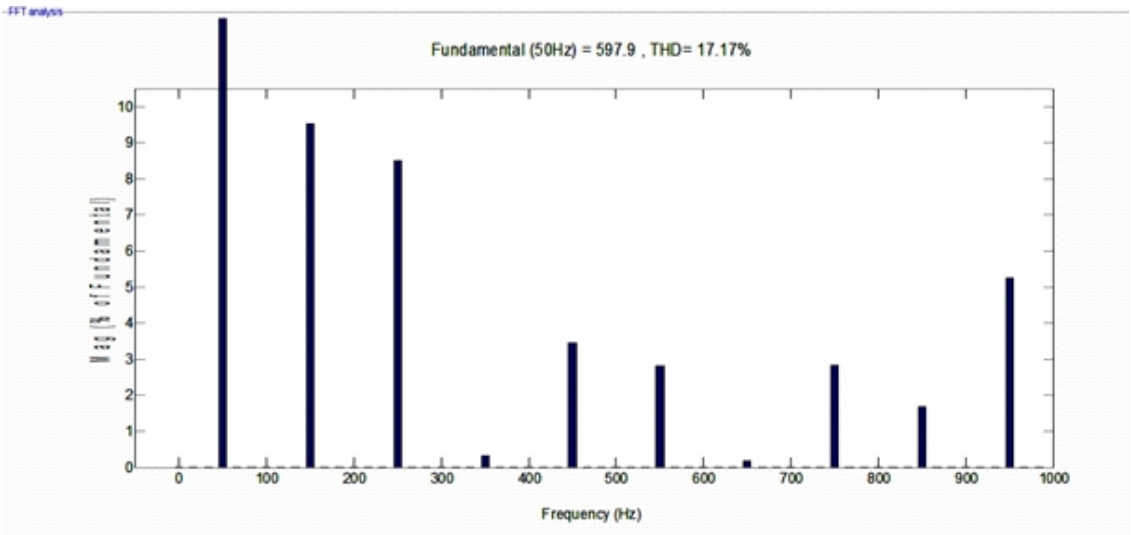

Figure 6. Harmonic spectrum of output voltage

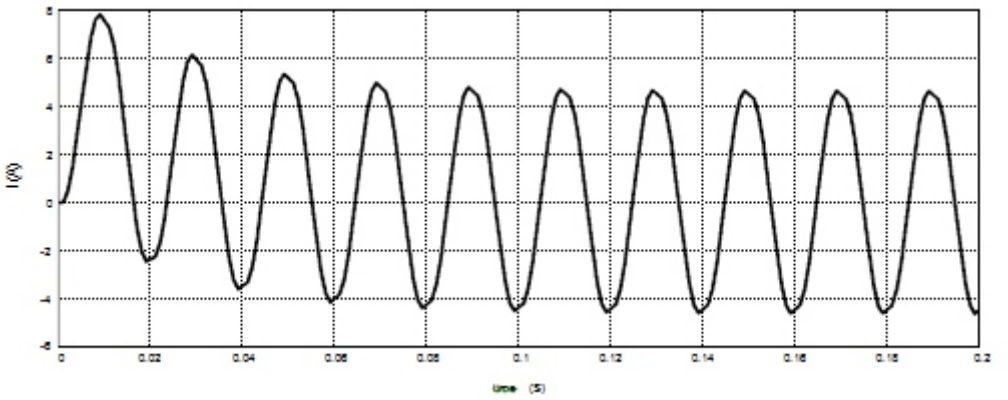

Figure 7. Load current

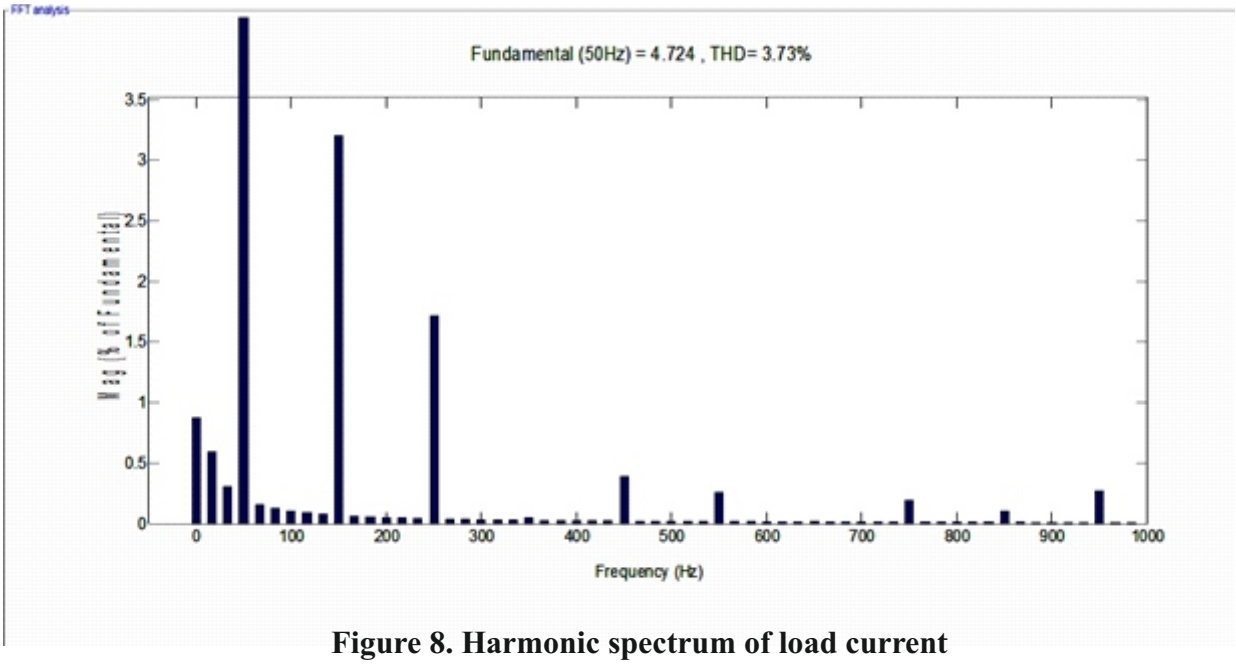

Figure 8. Harmonic spectrum of load current

VI. Conclusion

In this paper, a new structure has been proposed for symmetric cascaded multilevel inverter that has a simpler circuit and fewer power electronic components compared to the conventional cascaded inverter. The proposed inverter has been simulated by use of fundamental switching frequency and the results of the simulation confirm the performance accuracy of this inverter.

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