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Aims and Scope

Journal of Electrical Engineering and Advanced Technology is a journal that publishes original research papers in the fields of Electrical Engineering and Advanced Technology and in related disciplines. Areas included (but not limited to) are electronics and communications engineering, electric energy, automation, control and instrumentation, computer and information technology, and the electrical engineering aspects of building services and aerospace engineering, Journal publishes research articles and reviews within the whole field of electrical and electronic engineering, new teaching methods, curriculum design, assessment, validation and the impact of new technologies and it will continue to provide information on the latest trends and developments in this ever-expanding subject.

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Contents

Distance Control of Home Electric Applications Using GSM Module and at 89C2051 Microcontroller

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ABSTRACT

In this paper we describe the Distance control of Home Electric applications using GSM Module and AT 89C2051 microcontroller.This module can be extended to the any number of Electric applications by having an interface chip to 89C2051 microcontroller. Sending SMS through GSM modem when interfaced with microcontroller or PC is much simpler as compared with sending SMS through Modem in PDU Mode. Text message may be sent through the modem by interfacing only three signals of the serial interface of modem with microcontroller i.e., TxD, RxD and GND. When GSM module receives the message it sends the message in bit by bit form to the micro controller using UART. Now this micro controller sends signal to the ULN2003 Driver chip. Driver chip basically acts on open drain principle.To realize mobile control, 89C521 Microcontroller, electromagnetic relays, Driver circuit (ULM 2003) and GSM technologies for power management have been examined in this paper..

Key words: Distance Control, Home Electric applications, GSM Module, Short Message Service, Micro controller, AT 89C2051.

I .INTRODUCTION

The Global System for Mobile Communication (GSM) has become a very popular mode of communication. With mobile revolution in many third world countries like India opened up huge volume of working space for developing applications based on Mobile Services.

Distance control of Home Electric applications using GSM Module and AT 89C2051 microcontroller is one such application. Furthermore, to remotely control home appliances, the system to be developed would consists of a mobile phone and a microcontroller, which is characterized by input, and output terminals that can be utilized as communication channel to send message between the microcontroller and the devices being controlled. . As a result, GSM phone can be used in household power management to turn ON or OFF devices via a command in a Short Message Service (SMS) sending to the mobile phone connected to the automated device's controller.

The message is a data made up of address and command from microcontroller to the device being controlled. Conclusively, this paper is aimed at developing a GSM based Distance control of Home Electric applications could be used to remotely control for any number of electric applications using an interface chip.

II. BASIC CIRCUIT AND DESIGN

We designed a relay circuit using 89c51 microcontroller which could be switched on by single SMS to the device and can also be switched off by another SMS. Designed for control, this project provides 4 relay outputs. It can be used in various applications including load contact closure. The project presented here is based on world's most powerful Intel's mcs-51 family of microcontroller Atmel at89c51.In this project we are using AT 89C2051 microcontroller, because this controller has two ports which are more than enough for our project GSM modem is being interfaced with the microcontroller AT89s51 for SMS communication. The SMS can be sending for the control of devices. There are many applications of the project based on microcontroller 8051 and GSM interfacing. We can use it as a remote control of industrial machines or we can sue it for home automation or we can use it for the security of home or offices.

The sending SMS through GSM modem when interfaced with microcontroller or PC is much simpler as compared with sending SMS through Modem in PDU Mode. Text message may be sent through the modem by interfacing only three signals of the serial interface of modem with microcontroller i.e., TxD, RxD and GND. In this scheme RTS and CTS signals of serial port interface of GSM Modem are connected with each other. The transmit signal of serial port of microcontroller is connected with transmit signal (TxD) of the serial interface of GSM Modem while receive signal of microcontroller serial port is connected with receive signal (RxD) of serial interface of GSM Modem as shown in the Figure.1.

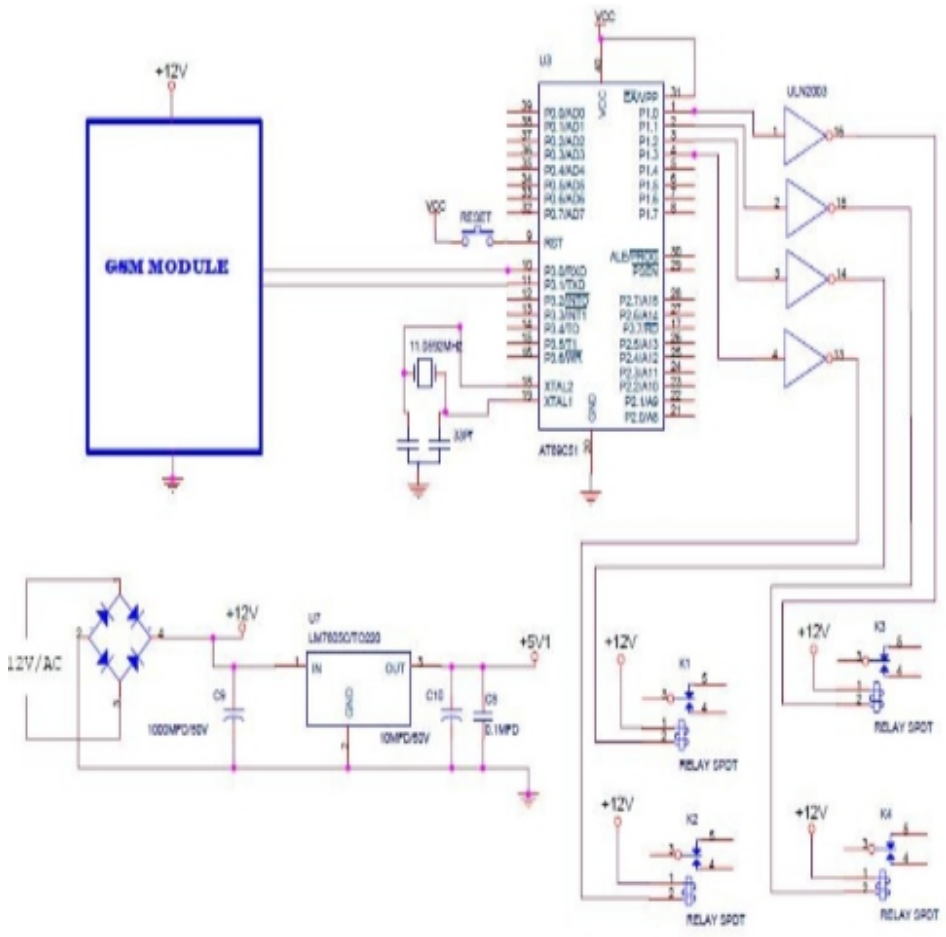

Fig. 1 Basic Circuit Diagram

III. CIRCUIT IMPLEMENTATION

The Power supply is taken through a step down transformer to decrease the voltage. This transformer gives 12V AC output. Diodes d1 to d4 are power rectifier diodes connected in bridge circuit c in circuit depicts the filter capacitor. Input to the bridge rectifier is transformer output which is12V AC. Output of the bridge rectifier and capacitor is 12V DC. All our relays are operated by 12V DC. Relay output can be connected to any 250V 7 ampere load. We should not cross this limit otherwise it will damage the relay circuit. 7805 regulator gets its input from the 12V DC power.5V DC is available at pin no 3 of this IC.c2 and c3 are filter capacitors ld1 is a power indication led IC2 is Atmel AT89c51 microcontroller. It has two ports port1 and port 3. This controller has inbuilt UART (Universal Synchronous, Asynchronous Receiver Transmitter), and pin no 10 is Rx pin and pin number 11 is Tx pin of the UART. Through these two pins microcontroller is able to communicate with the GSM sim module through UART.

UART is described as Universal Asynchronous Receiver/Transmitter. This is a type of "asynchronous receiver/transmitter", a piece of computer hardware that translates data between parallel and serial forms. UARTs are commonly used in conjunction with communication standards such as EIA, RS-232, RS-422 or RS-485. The universal designation indicates that the data format and transmission speeds are configurable and that the actual electric signaling levels and methods (such as differential signaling etc.) typically are handled by a special driver circuit external to the UART.

A UART is usually an individual (or part of an) integrated circuit used for serial communications over a computer or peripheral device serial port. UARTs are now commonly included in microcontrollers. A dual UART or conversion between serial and parallel forms. Serial transmission of digital information (bits) through a single wire or other medium is much more cost effective than parallel transmission through multiple wires.

The UART usually does not directly generate or receive the external signals used between different items of equipment. Separate interface devices are used to convert the logic level signals of the UART to and from the external signaling levels. External signals may be of many different forms. Examples of standards for voltage signaling are RS-232, RS-422 and RS-485.

IV. WORKING PROCEDURE

The working of the whole project is described below:

We have to send message to the Sim in GSM module in forms of 1's and 0's, this is nothing but we are sending the message in form of binary digits. Each bit represents each device connected through the circuit. For example if we send 1101 as message then the hard ware will switch on the 1st, 2nd, and 4th devices and turns off the 3rd device. Like this we can control the whole set up by sending 1's and 0's which means on and off respectively.

The micro controller runs as per the program installed in it. This program is written in C language and compiled using keil compiler. Now this program is installed in the microcontroller using u programmer.

When GSM module receives the message it sends the message in bit by bit form to the micro controller using UART Now this micro controller sends signal to the ULN2003 Driver chip. Driver chip basically acts on open drain principle.

An open collector is a common type of output found on many integrated circuits (IC). Instead of outputting a signal of a specific voltage or current, the output signal is applied to the base of an internal NPN transistor whose collector is externalized (open) on a pin of the IC. The emitter of the transistor is connected internally to the ground pin. If the output device is a MOSFET the output is called open drain and it functions in a similar way.

DUART combines two UARTs into a single chip. Many modern ICs now come with a UART that can also communicate synchronously; these devices are called USARTs (universal synchronous/asynch ronous receiver/transmitter).

The Universal Asynchronous Receiver/Transmitter (UART) takes bytes of data and transmits the individual bits in a sequential fashion. At the destination, a second UART re-assembles the bits into complete bytes.

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In figure 2, the transistor base is labeled "IC Output". This is an internal output from the internal IC logic to the transistor. From the point of view of the transistor, this is the input which controls the transistor switching. The external output is the transistor collector, and the transistor acts as an interface between the internal IC logic and parts external to the IC.

The output essentially acts as either an open circuit (no connection to anything) or a connection to ground. The output has a pull-up resistor, which raises the output voltage when the transistor is turned off. When the transistor connected to this resistor is turned on, the output is forced to nearly 0 volts.

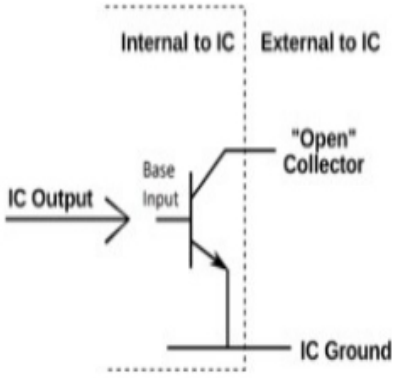

Fig. 2. Open Drain System

The output is fed to SPDT Relay. There are 3 poles for this pcb spdt relay, two are for forming the control circuit and the remaining one acts as a switch by making and losing the contact with the circuit. The two terminals of the controlling circuit are connected with the driver chip output and 12V supply. Phase voltage is connected to the lamp circuit through the relays, so now when the relay makes contact the bulbs glow and when it loses the contact it gets off. Driver chip operates such that the output is at 0V i.e.., grounded state or in open state. Hence when it gives 0V the circuit is completed and the relay operates, the bulbs glow. If it gives the output as open circuit then the bulb goes off. In this way the hardware device controls the supply.

V. SOFTWARE IMPLEMENTATION

The micro controller runs as per the program installed in it. This program is written in C language and compiled using keil compiler. Flow chart as shown in the figure 3.

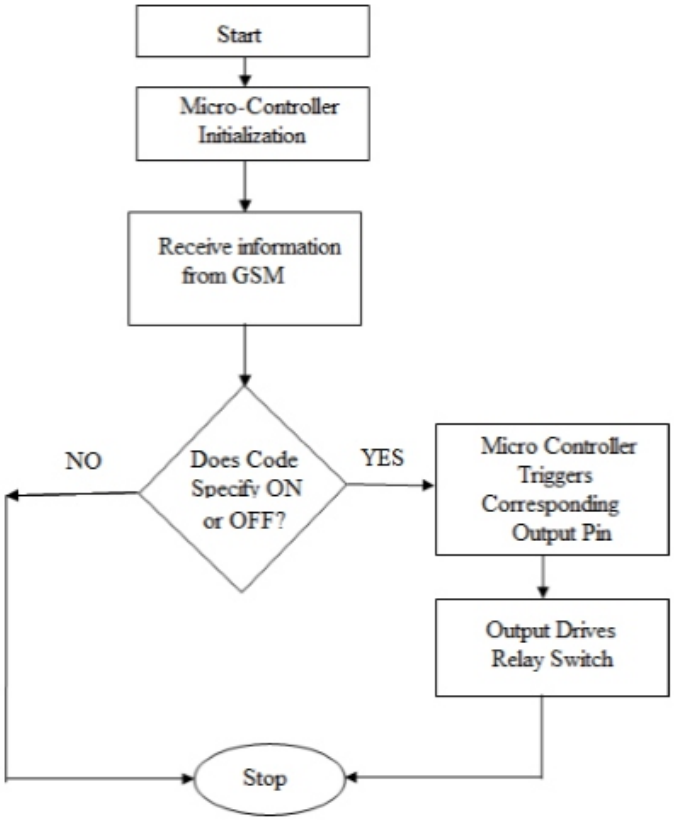

Fig. 3. Flow-chart

VI. RESULTS

Sample Case at home with four electric applications:
Average time during which Electrical appliances are left running: 5 hrs per day Average power consumption during the above time:
Average power consumed by Tube light: (40 watts /0.9 + 40) = 85 Watts per hour Average Power consumed by Fan: 50 watts per hour
Average Power consumed by laptop: 100 Watts per hour
Average power consumed by Geyser: 3000/10=300 watts per hour
Total Power wastage in a day = (85+50+100+300=535 watts per hr * 5 hrs per day)
=2675 watts or 2.675 KWh or 2.675 units of electricity

Money spent on purchasing this power = 5.3*2.675 = Rs 14.1775/- Cost of installation = Rs 6500/-
Payback time (Time during which the installation costs are recovered) = 6500/14.1775 = 458.472 days or 1.25 years

VII. CONCLUSIONS

In this project a mobile-controllable power outlet system and the key components for home power management have been developed. To realize mobile control, 89C521 Microcontroller, electromagnetic relays, Driver circuit (ULM 2003) and GSM technologies for power management have been integrated. The proposed MPCOM is designed for wireless controlling of different electric home appliances connected over a GSM network in a domestic environment.

The MPCOM also a GSM cellular mobile phone using SMS and PC or Notebook using the Internet control electric home appliances at remote locations. The experiments and the analysis reported in this project have demonstrated that this new system can be practically implemented and provides adequate results. While this study has its limitations, it is hoped that it will serve as a basis for further study of home power management strategies for various electric home appliances.

Home power management is required to save energy and reduce carbon dioxide emissions. With burgeoning prices and depleting resources effective power management and home automation provide a good alternative. The device can be scaled to integrate various other technologies like Bluetooth, Infrared, RF technologies to achieve similar results. Miniaturization of the entire hardware kit and its development and cost-effective production is imperative to encourage the idea of home automation in the Indian power sector. Minimization and optimal power consumption by the device is also a challenge that needs to be addressed in the future versions of this device.

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A View of Glucose Detector, Oxygen Sensor and Blood Pressure Sensor in Biochips

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ABSTRACT

"Biochips"-The most exciting future technology is an outcome of the fields of Computer science, Electronics & Biology. It's a new type of bio-security device to accurately track information regarding what a person is doing, and who is to accurately track information regarding what he is doing, and who is actually doing it. It's no more required with biochips the good old idea of remembering pesky PINs, Passwords, & Social security numbers .No more matters of carrying medical records to a hospital, No more cash/credit card carrying to the market place; everything goes embedded in the chip…. Everything goes digitalized. No more hawker tricks on the internet….! Biochip has a variety technique for secured E-money transactions on the net. The power of biochips exists in capability of locating lost children, downed soldiers, and wandering Alzheimer patients.

Our contributions to this paper lie in the aspects of "Implementation of Glucose detector in Biochips" "Implementation of Oxygen sensor in Biochips" "Implementation of Blood pressure sensor in Biochips"

"Proposal of Solution for the typical theft problem faced by the Biochips"

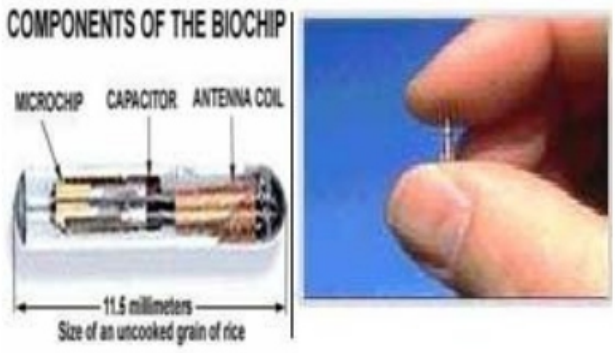
The four contributions have been discussed in detail with the proposed principles for implementation of the concepts.

INTRODUCTION

Biochips are any microprocessor chips that can be used in Biology. The biochip technology was originally developed in 1983 for monitoring fisheries, it's use now includes, over 300 zoos, over 80 government agencies in at least 20 countries, pets (everything from lizards to dogs), electronic "branding" of horses, monitoring lab animals, fisheries, endangered wildlife, automobiles, garment tracking, hazardous waste, and humans. Biochips are "silently" inching into humans. For instance, at least 6 million medical devices, such as artificial body parts (prosthetic devices), breast implants, chin implants, etc., are implanted in people each year. And most of these medical devices are carrying a "surprise" guest — a biochip. In 1993, the Food and Drug Administration passed the Safe Medical Devices Registration Act of 1993, requiring all artificial body implants to have "implanted" identification — the biochip. So, the yearly, 6 million recipients of prosthetic devices and breast implants are "biochipped". To date, over 7 million animals have been "chipped". The major biochip companies are A.V.I.D. (American Veterinary Identification Devices), Trovan Identification Systems, and Destron-Fearing Corporation.

The Biochip Technology

The current, in use, biochip implant system is actually a fairly simple device. Today's, biochip implant is basically a small (micro) computer chip, inserted under the skin, for identification purposes. The biochip system is radio frequency identification (RFID) system, using low-frequency radio signals to communicate between the biochip and reader. The Biochip Implant System Consists Of Two Components:



Perspective of the Actual Size

The Transponder:

The transponder is the actual biochip implant. It is a passive transponder, meaning it contains no battery or energy of its own. In comparison, an active transponder would provide its own energy source, normally a small battery. Because the passive biochip contains no battery, or nothing to wear out, it has a very long life, up to 99 years, and no maintenance. Being passive, it's inactive until the reader activates it by sending it a low-power electrical charge. The reader "reads" or "scans" the implanted biochip and receives back data (in this case an identification number) from the biochip. The communication between biochip and reader is via low-frequency radio waves.

The biochip transponder consists of four parts:

1. Computer Microchip: The microchip stores a unique identification number from 10 to 15 digits long. The storage capacity of the current microchips is limited, capable of storing only a single ID number. AVID (American Veterinary Identification Devices), claims their chips, using an nnn-nnn-nnn format, has the capability of over 70 trillion unique numbers. The unique ID number is "etched" or encoded via a laser onto the surface of the microchip before assembly. Once the number is encoded it is impossible to alter. The microchip also contains the electronic circuitry necessary to transmit the ID number to the "reader".

2. Antenna Coil: This is normally a simple, coil of copper wire around a ferrite or iron core. This tiny, primitive, radio antenna "receives and sends" signals from the reader or scanner.

3. Tuning Capacitor: The capacitor stores the small electrical charge (less than 1/1000 of a watt) sent by the reader or scanner, which activates the transponder. This "activation" allows the transponder to send back the ID number encoded in the computer chip. Because "radio waves" are utilized to communicate between the transponder and reader, the capacitor is "tuned" to the same frequency as the reader.

4. Glass Capsule: The glass capsule "houses" the microchip, antenna coil and capacitor. It is a small capsule, the smallest measuring 11 mm in length and 2 mm in diameter, about the size of an uncooked

grain of rice. The capsule is made of biocompatible material such as soda lime glass. After assembly, the capsule is hermetically (air-tight) sealed, so no bodily fluids can touch the electronics inside. Because the glass is very smooth and susceptible to movement, a material such as a polypropylene polymer sheath is attached to one end of the capsule. This sheath provides a compatible surface which the bodily tissue fibers bond or interconnect, resulting in a permanent placement of the biochip.

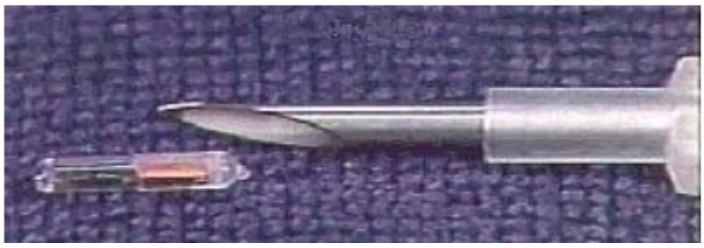


Fig: Biochip and Syringe

The biochip is inserted into the subject with a hypodermic syringe. Injection is safe and simple, comparable to common vaccines. Anesthesia is not required nor recommended. In dogs and cats, the biochip is usually injected behind the neck between the shoulder blades. Trovan, Ltd., markets an implant, featuring a patented "zip quill", which you simply press in, no syringe is needed. According to AVID "Once implanted, the identity tag is virtually impossible to retrieve.
. . The number can never be altered."

The Reader:
The reader consists of an "exciter" coil which creates an electromagnetic field that, via radio signals, provides the necessary energy (less than 1/1000 of a watt) to "excite" or "activate" the implanted biochip. The reader also carries a receiving coil that receives the transmitted code or ID number sent back from the "activated" implanted biochip. This all takes place very fast, in milliseconds. The reader also contains the software and components to decode the received code and display the result in an LCD display. The reader can include a RS-232 port to attach a computer.

Working of a Biochip: The reader generates a low-power, electromagnetic field, in this case via radio signals, which "activates" the implanted biochip. This "activation" enables the biochip to send the ID code back to the reader via radio signals. The reader amplifies the received code, converts it to digital format, decodes and displays the ID number on the reader's LCD display. The reader must normally be between 2 and 12 inches near the biochip to communicate. The reader and biochip can communicate through most materials, except metal.

THE APPLICATIONS:
With a biochip tracing of a person/animal, anywhere in the world is possible: Once the reader is connected to the internet, satellite and a centralized database is maintained about the biochipped creatures, It is always possible to trace out the personality intended.

A biochip can store and update financial, medical, demographic data, basically everything about a person: An implanted biochip can be scanned to pay for groceries, obtain medical procedures, and conduct financial transactions. Currently, the in use, implanted biochips only store one 10 to 15 digits. If biochips are designed to accommodate with more ROM & RAM there is definitely an opportunity.

A biochip leads to secured E-Commerce systems: It's a fact; the world is very quickly going to a digital or E-economy, through the Internet. It is expected that by 2008, 60% of the Business transactions will be performed through the Internet. The E-money future, however, isn't necessarily secure. The Internet wasn't built to be Fort Knox. In the wrong hands, this powerful tool can turn dangerous. Hackers have already broken into bank files that were 100% secure. A biochip is the possible solution to the "identification and security" dilemma faced by the digital economy. This type of new bio-security device is capable of accurately tracking information regarding what users are doing, and who are to accurately track information regarding what users are doing, and who is actually doing it.

Biochips really are potent in replacing passports, cash, and medical records: The really powered biochip systems can replace cash, passports, medical & other records! It's no more required to carry wallet full cash, credit/ATM cards, passports & medical records to the market place. Payment system, authentication procedures may all be done by the means Biochips.

Medicinal implementations of Biochips: A New Era Proposed by us Biochip as Glucose Detector: The Biochip can be integrated with a glucose detector. The chip will allow diabetics to easily monitor the level of the sugar glucose in their blood. Diabetics currently use a skin prick and a hand-held blood test, and then medicate themselves with insulin depending on the result. The system is simple and works well, but the need to draw blood means that most diabetics don't test themselves as often as they should. Although they may get away with this in the short term, in later life those who monitored infrequently suffer from blindness, loss of circulation, and other complications. The solution is more frequent testing, using a less invasive method. The biochip will sit underneath the skin, sense the glucose level, and send the result back out by radio- frequency communication.

Proposed principle of Glucose detection: A light-emitting diode (LED) in the biochip starts off the detection process. The light that it produces hits a fluorescent chemical: one that absorbs incoming light and re-emits it at a longer wavelength. The longer wavelength of light is then detected, and the result is sent to a control panel outside the body. Glucose is detected because the sugar reduces the amount of light that the fluorescent chemical re-emits. The more glucose there is the less light that is detected.

Biochip as Oxygen sensor : The biochip can also be integrated with an oxygen sensor .The oxygen sensor will be useful not only to monitor breathing in intensive care units, but also to check that packages of food, or containers of semiconductors stored under nitrogen gas, remain airtight. Proposed principal of Oxygen sensor in Biochip: The oxygen-sensing chip sends light pulses out into the body. The light is absorbed to varying extents, depending on how much oxygen is being carried in the blood, and the chip detects the light that is left. The rushes of blood pumped by the heart are also detected, so the same chip is a pulse monitor.

Biochip as a Blood Pressure sensor: In normal situations, The Blood Pressure of a healthy Human being is 120/80 mm of Hg. A Pressure ratio lower than this is said to be "Low BP " condition & A Pressure ratio more than this is "High BP" condition. Serious Effects will be reflected in humans during Low & High BP conditions; it may sometimes cause the death of a Person. Blood Pressure is checked with BP Apparatus in Hospitals and this is done only when the patient is abnormal. However, a continuous monitoring of BP is required in the aged people & Patients. A huge variety of hardware circuitry (sensors) is available in electronics to detect the flow of fluid. It's always possible to embed

this type of sensors into a biochip. An integration of Pressure (Blood Flow) detecting circuits with the Biochip can make the chip to continuously monitor the blood flow rate & when the pressure is in its low or high extremes it can be immediately informed through the reader hence to take up remedial measures.

Typical Problem of Biochips: A Solution Proposed –

The Lock: Problem before the world a chip implant would contain a person's financial world, medical history, health care — it would contain his electronic life". If cash no longer existed and if the world's economy was totally chip oriented; — there would be a huge "black-market" for chips! Since there is no cash and no other bartering system, criminals would cut off hands and heads, stealing "rich-folks" chips. "It is very dangerous because once kidnappers get to know about these chips, they will skin people to find them," (New York Times, June 20, 1999) The typical solutions won't work well are already proposed by different people: The Biochip must retain data only if it is placed in a fluid medium like blood & not in any other medium. This technique is unsuitable for identification of dead bodies (murdered by the kidnappers) as it loses the data about the social security number. The data in the Biochip must be erased if it is exposed to sunlight/air. This technique is unsuitable as transplantation of biochip from genuine to the fraud in darkness (by means of infrared light) or in the vacuum (by means of oxygen cylinders). And many such…….!!!!!!!!

Our key: The solution Proposed by us a generic & existing model of Biochips consists of only ROM component in it and is capable of accommodating the data such as social security number, Passport number, bankcard number etc., which are normally permanent in nature. The induction of RAM component in addition to ROM & storing the Bankcard, Financial details which causes the problem is a mere solution. As RAM needs to be continuously charged in order to retain the data, Current can be supplied to the chip either from the electrical energy produced in the cells or by converting the heat energy in our body to electrical energy. Once if the chip is taken out from the human body RAM immediately loses the Power supply from the human body; thus information in the RAM is lost and therefore is useless for the kidnappers. However this technique will not affect the data in ROM i.e. Social security number that can be used to detect the address of the dead bodies that were unidentified.

CONCLUSION

The Cyber Future InfoTech will be implanted in our bodies. A chip implanted somewhere in human bodies might serve as a combination of credit card, passport, driver's license, personal diary. No longer would it be needed to worry about losing the credit cards while traveling. A chip inserted into human bodies might also give us extra mental power. The really fascinating idea is under fast track research "but we're close." The day in which we have chips embedded in our skins is not too far from now. "This is science fiction stuff.", "This is a true example to prove science really starts with fiction".

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Clock Gated Low Power 64- BIT Register Design

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ABSTRACT

We achieve 25% power reduction in clock gated 64-bit Register design when we provide clock period of 2 ns to 64-bit register. We again achieve 16.66% power reduction in 64-bit Register when we provide clock period of 2 ns to 64-bit register. Clock gating reduces dynamic power dissipation in 64-bit register but increases junction temperature of device. Xilinx planahead 14.1 is used as simulator and Virtex-6 is used as 40-nm FPGA device for implementation purpose. We apply clock gate to inhibit clock when device is not in use, in order to reduce power dissipation.

Keywords—Sequential Circuit, Low Power, Clock Gating, Glich Free Design, Register Transfer Level, Register, LUT, Buffer.

I. INTRODUCTION

Dynamic power consists of clock power along with signal power, IOs power and logic power. Only Clock power contributes 45-60 percent of total dynamic power. Hence, reducing clock power is very important. In order to reduce clock power dissipation, we design a small circuit called clock gate. Clock gate is a logic gate which takes clock in form of input and produce gated clock in form of output.
ClockGate = Clock + Gate(either ANDor OR)

It has 2 instances and 3 nets. When ctr is logic low then it prohibit supply of clock and gated off the device and reduce power dissipation too.

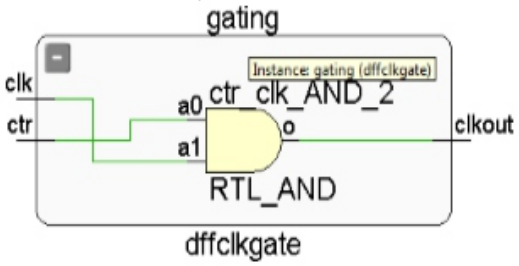

Figure 1: Schematic of Clock Gate

Clock Gated 64-bit Register contains 3 Instances, 131 input or output ports and 135 nets. A net is a set of interconnected pins and wires. Every wire has a net name, which identifies it to the Schematic and Symbol Editors and netlister programs. Two or more wires can have the same net name. In a net, all wire share the same name and all symbol pins connected to these wires are electrically connected. Buses are a convenient way to group related signals. However, buses can be any group of signals, related or not.

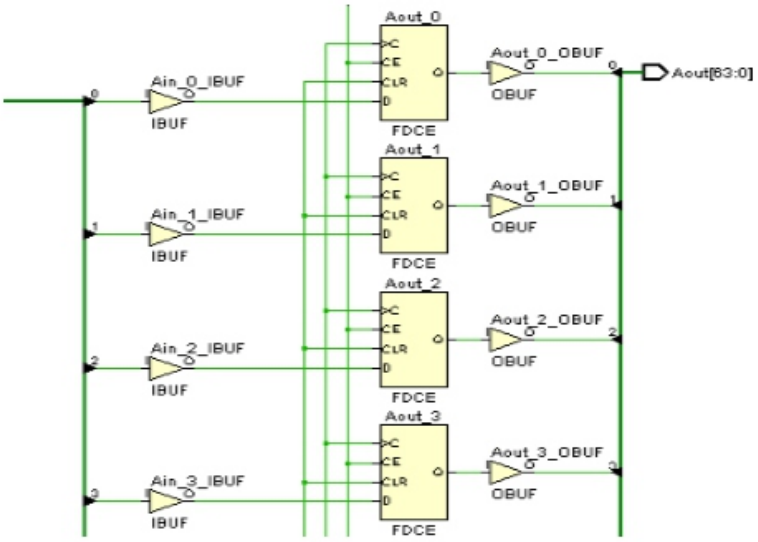

Figure 2: Schematic of 64-bit Register Aout_0-Aout_63

This Register has 64 D flip-flop. First D flip-flop is Aout_0 and last flip-flop is Aout_63. Aout_0 has one input buffer called Ain 0. Aout 0 has one output buffer called Aout 0.

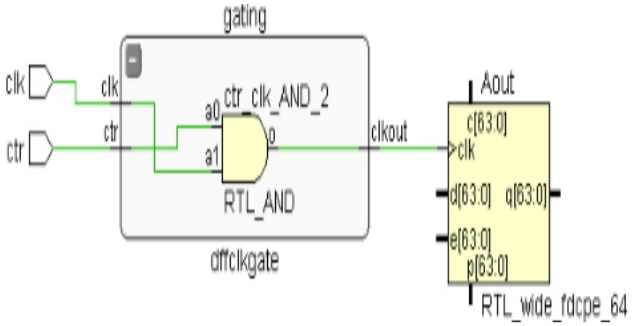

Figure 3: Application of Clock Gate to 64-bit Register

We apply clock gate to 64-bit register in order to reduce dynamic power consumption of register. If ctr is 0 then clk will not reach to register and register will switched off. When register is in off state, it will not consume power. In that way, we achieve our goal of power saving. Area is a trade-off in this technique. Using Clock gating, we decreases clock power, signal power but increases IO power and ineffective in case of leakage power.

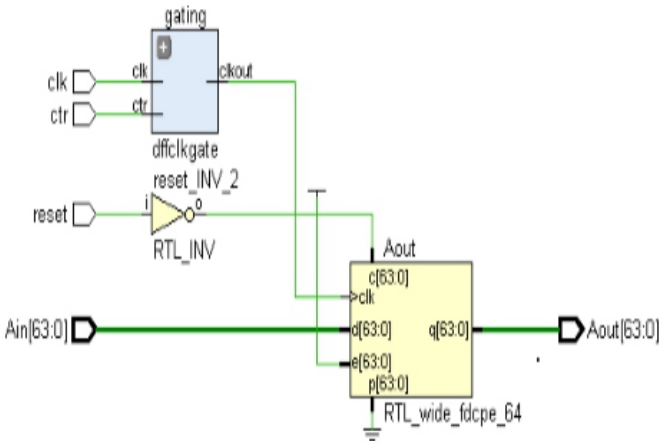

Figure 4: Clock Gated Low Power 64-Bit Register Design

II. RELATED WORK

In reference [1], clock gating techniques such as Valid Clock Gating, Idle State Based Clock Gating and Observability don't care based Clock Gating are three techniques to achieve reduction in power consumption. Idle state based clock gating is taken into consideration when the current state value and the next state value of an FF are the same, it is unnecessary for the FF to transmit the next state value in the next clock cycle. Therefore, it is valid to freeze the FF under such situation. Observability don't cares (ODC) of a Boolean variable are the conditions under which the variable is not affecting any of the primary outputs (PO). If the next state value cannot be observed in the coming clock cycles, the FF can be clock gated in those clock cycles. Works in [1], extended the theory of determining valid clock gating conditions to cover originally invalid conditions for more power savings. And [1] also introduced a procedure of finding error cancellation based clock gating conditions. In paper [2], Latch-free based design; Latch-based design and Flip-flop based design are many clock gating styles available to optimize power in VLSI circuits. According to [2], paper raise issues in implementation of clock gating design techniques. The clock gate (i.e., AND or OR) must not alter the waveform of the clock other than switching the clock on or off is first issue. Clock gating holds time violations and set-up time violations can be fixed like other violations during physical design phase is other issue in clock gating. Reference [2] proposes some techniques which can used to fix hold violations are clock skewing/buffering in data path near to endpoint. The main motive of [2] deals with Glitches-transient fault, which occur due to design error. Techniques in [3], achieved 93.75% clock power reduction in ALU. Reduction of power consumption in ALU helps us to realize low power processor. [3] Deals with the design and implementation of a Clock Gating Aware Low Power Arithmetic and Logic Unit that has been developed as part of low power processor. In [3], our designed ALU has 16 functions. Each function has one dedicated module. When one instruction executes in their respective module. Others module that was not used by current executing instruction must gated off by the clock gate. From given formula,

$$Power \quad \text{Re}\, duction \quad \% = \frac{Number\ of\ Unit \qquad Gated}{Total\ Number \quad of\ Unit} * 100$$

Here, when any one of module execute because of clock gating rest 15 modules turned off and hence reduce power (15/16)*100=93.75% power reduction. Reference [4] reveals a large margin of potential for power saving based on clock gating functions that initially appear to be useless due to timing violation or excessive power consumption. Two optimization techniques is proposed in [4] for resurrecting such functions that can be used as a generic post-processing phase in an automatic clock gating tool. The first provides timing-aware approximation and the second aims at generating large gating domains by clustering similar clock gating functions.

III. RESULTS

A. Top-Level Schematic of 64-bit Register

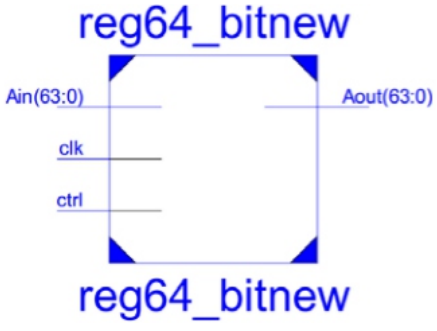

Figure5: Top Level Schematic of 64-bit Register

It has one 64-bit input Ain. Clock and control are two others outputs. It has one 64-bit output Aout. Register is a circuit which store information. This 64-bit register stores 64-bit inputs.

B. RTL Schematic of 64-bit Register

RTL is Register Transfer Level schematic. That display how this design will transfer on register in next phase of synthesis and implementation. It is based on native generic register (NGR) file. NGR was earlier EDIF in electronics. It uses 65 D flip-flop and one AND gate.

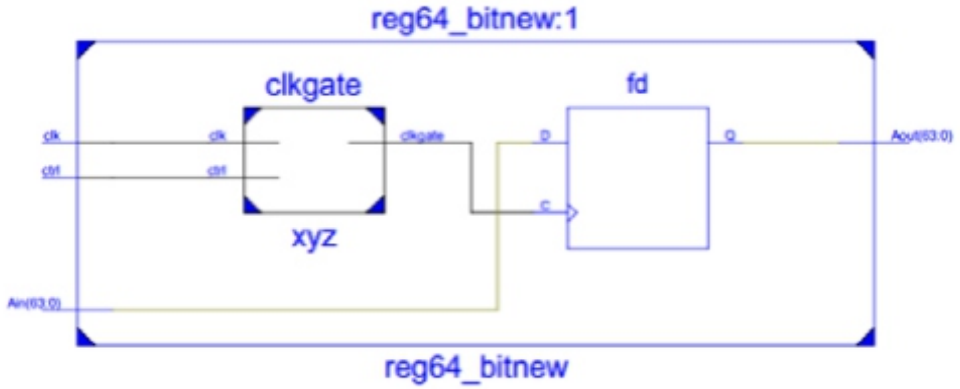

Figure6: RTL schematic of 64-bit Register

Depending on control condition clock gate will control the supply of clock to registers. When ctrl is high, then clock will be provided to register. Otherwise, we prohibit clock to register.

C. Top Level Schematic of Clock Gate

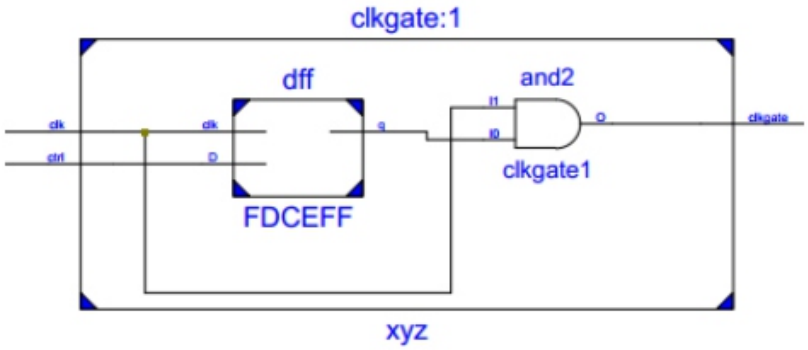

Figure7: Top Level Schematic of Clock gate

Clock gate is a combination of logic gate AND/OR and D Flip-Flop. First, D Flip-flop delay to reach control or enable to logic gate. Then the value of control or enable signal determine clock will be provided to register or not.

D. Technology Schematic of Clock Gate

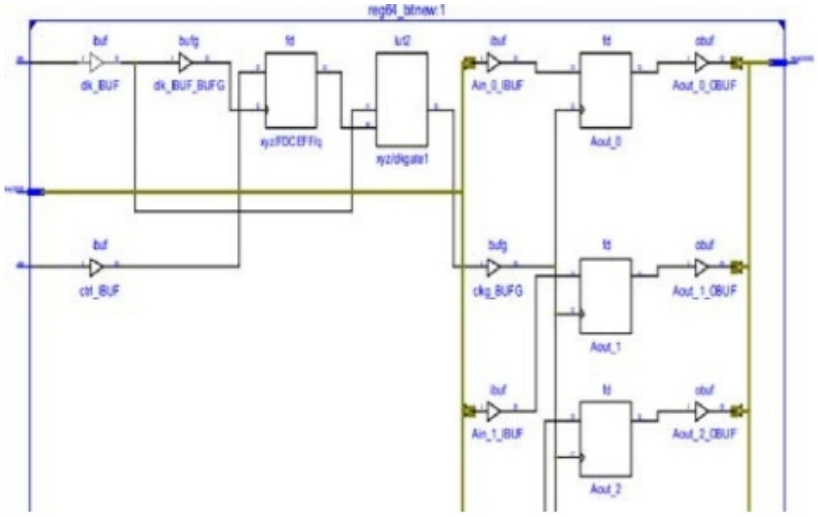

Figure8: Technology Schematic of 64-bit Register (a)

Above Figure shows 4 Flip-Flops. One flip-flop is used in clock gate circuits. Three flip-flops is used in register circuits.

It consists of one LUT2, 65 D Flip-Flops, one in clock gate and 64 in registers. It has two global clock buffers. It has 130 buffers. Out of 130, 66 are input buffer and 64 are output buffers

Figure9: Technology Schematic of 64-bit Register (b)

Technology Schematic is based on native generic circuit(NGC) file. It shows the netlist based on LUT and gate. This schematic has one two-input look up table.

E. Power Consumption

Power dissipation has two components. One is dynamic power and other is static power. In this analysis on XPower, dynamic power consists of clock power, logic power, signal power and IOS power. Static Power is also called Leakage Power.

Power Consumption with Clock Gate			
	15ps	2ns	15ns
Clock Power	1.351W	0.008W	0.002W
Logic Power	0.019W	0.000W	0.000W
Signal Power	0.505W	0.004W	0.001W
IOs Power	36.679W	0.132W	0.022W
Leakage Power	0.773W	0.043W	0.042W

Power Consumption is inversely proportional to clock period and directly proportional to clock frequency. It is maximum at 15ps clock period. It is minimum at 15ns.

F. Dynamic Current

It is the current, which our device takes, when our design register is in use.

Power Consumption with Clock Gate			
	15ps	**2ns**	**15ns**
Vccint	3.777A	0.020A	0.004A
Vccaux	1.996A	0.007A	0.001A
Vcc018	17.325A	0.062A	0.010A
Vccbram	0.000A	0.000A	0.000A

Dynamic current is affected by these above four voltages. These are Vccint, Vccaux, Vcc018 and Vccbram. Dynamic current is affected with minor variation in clock period.

G.Static Current

Static current is leakage current, which flow only when device is in off state. In real life, we face with this problem, when our mobile discharge after a couple of day, even if we don't use our cell phone.

Power Consumption with Clock Gate			
	15ps	2ns	15ns
Vccint	0.625A	0.017A	0.017A
Vccaux	2.063A	0.013A	0.013A
Vcc018	17.326A	0.001A	0.001A
Vccbram	0.025A	0.000A	0.000A

Static current is not affected with minor variation in clock period. Vccint is supply for the core unit. Vccaux is supply for the configuration pins and unit. Vcco is supply for the IO buffers.

H.Effect on Temperature

Junction Temperature with and w/o Clock Gating			
Junction Temperature	15ps	2ns	5ns
Without Clock Gate	125^0C	25.6^0C	25.2^0C
With Clock Gate	-----	25.9^0C	25.3^0C

Clock Gating is a technique, which decreases power consumptions but increases junction temperature.

I. Effect on Clock Gate

On 2 ns	With Clock Gate	Without Clock Gate
Clock Power	0.007W	0.008W
Signal Power	0.003W	0.004W
Total Power	10mW	12mW

We achieve 16.66% power reduction in 64-bit Register when clock period is 2 ns in 64-bit register. In this way, we achieve our prime goal to reduce consumption of power in our design.

On 5 ns	With Clock Gate	Without Clock Gate
Clock Power	0.002W	0.003W
Signal Power	0.001W	0.001W
Total Power	3mW	4mW

We achieve 25% power reduction in 64-bit Register when we provide clock period of 2 ns to 64-bit register.

IV. CONCLUSION

16.66% clock and signal power reduction in 64-bit Register when we provide clock period of 2 ns to 64-bit register. 25% clock and signal power reduction in 64-bit Register when we provide clock period of 2 ns to 64-bit register. Power reduction is benefit of clock gating techniques but area is trade off of this technique which increases due to additional clock circuitry. Another trade-off is Temperature. Temperatures slightly increase with significant decrease in power consumptions.

V. FUTURE SCOPE

This implementation is on 40-nm Virtex-6 FPGA. Now, there is scope to implement clock gated sequential circuit on latest 28-nm Virtex-7, Artix-7 FPGA. There is a scope to implement clock gate on the larger circuit in order to reduce power dissipation in significant amount.

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Load Voltage Regulation using Modified Switching Controller based DVR

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A B S T R A C T

The main objective of paper is three-phase four-wire DVR with modified switching band controller topology is proposed, which overcomes the frequent band violation, poor controllability and heavy filter currents compared to three- phase four wire DVR with conventional filter topology. In a modified switching band controller DVR, the performance of the controller depends on the values of filter components. After modified switching controller based Dynamic voltage restorer (DVR). The DVR is to mitigate all typical voltage related problems at the distribution system load center like voltage sag, voltage swell, voltage harmonics and interruptions etc. The compensation capability of this proposed topology is analyzed based on simulation studies and corresponding results are compared with different switching control strategies. The consequent merits and demerits of switching loss in VSI ripple in compensated load voltages and error between reference injected voltages and actual injected voltages in different switching control strategies are discussed. Total harmonic distortions THDs (%) of compensated load voltages, PCC voltages and source voltages are also presented.

Keywords: Dynamic voltage restorer (DVR); Fixed hysteresis band controller; Adaptive hysteresis bandcontroller; Modified switching band controller; Total harmonic distortion (THD).

1. INTRODUCTION

Now a day, power quality is the major concern in power system network. The wide usage of modern power electronic equipments, frequent starting and stop of induction dives and integration of renewable energy sources etc. causes power quality (PQ) problems[1]-[6]. The well known power quality issues are voltage sag/swell, harmonic content in voltage and current and so on. To mitigate these PQ issues custom power devices (CPDs) are used [7]-[9]. In distribution grid these CPDs can be connected in series or in parallel or combination of both at the point of common coupling (PCC). Dynamic voltage restorer (DVR) is one of the series connected type CPD.DVR consists of voltage source inverter (VSI) connected between load and PCC through coupling transformer and interface filter. Hence the DVR injects a set of controllable three- phase ac voltages in series and synchronism with the distribution feeder voltages such that the load-side voltage is restored to the desired amplitude and waveform even when the source voltage is unbalanced or distorted. In this paper primary aspect is the design of DVR for the selection of suitable VSI topology based on the nature of load and network configuration. Three phase neutral clamped VSI topology is shown in Fig.1 is used. It consists of six power semiconductor switches each with an anti-parallel diode and two identical DC storage capacitors. This topology enables the independent control of each leg of the series inverters, but it requires capacitor voltage balancing [10]. In [11]-[13], four-leg VSI topology for series active filter has been proposed for a three-phase four-wire system. This topology avoids the voltage balancing of the capacitor, but the independent control of the inverter legs is not possible. To overcome the problems

associated with the four-leg topology, this topology is equipped to compensate DC components of load also, but due to the presence of DC component in VSI, the two DC capacitors are charged to different voltages. The total voltages of DC capacitors are however maintained at a constant value using a DC voltage control loop. Hence, with the presence of DC component in load, an extra circuitry and appropriate changes in control are required to maintain individual DC voltages at constant value. The second aspect is the design of DVR for the selection of suitable coupling transformer[8], it can experience saturation during the transient period after a voltage sag starts. For preventing this, normally a rating flux that is double of the steady-state limit is chosen. An alternative method for preventing the coupling transformer saturation based on limiting the flux-linkage during the transient switch-on period is proposed in [14] -[15]. The DVR coupling transformer performs two important functions: voltage boost and electrical isolation. The third aspect is the design of DVR for the selection of suitable interface inductor (Lf), DC capacitor storage series resistance (Rse) and the capacitance (Cse).

2. CONVENTIONALTHREE-PHASE FOUR WIRE DVR TOPOLOGY

Schematic of conventional three phase three leg-four wire DVR topology is shown fig.1 This topology consists of voltage source inverter (VSI) connected in series to load at the PCC through coupling transformer, interface filter (interface inductor (Lse) and capacitor (Cse)). The purpose of interfacing filter is to shape inject voltages while tracking the reference injected voltages. Here v_{la}, v_{lb}, v_{lc} represents the instantaneous phase voltages at the PCC, which may be distorted because of faults that can exist in the system are single line-to-ground fault, double line-to- ground, line-to-line fault and three-phase fault. The injected voltages v_{inja}, v_{injb}, v_{injc} represents the actual injected voltages obtained using hysteresis current control techniques i_{sa}, i_{sb}, i_{sc} represents the source currents and i_{la}, i_{lb}, i_{lc} represents the load currents. The capacitance C_{dc} is the dc storage capacitor used for maintaining the input voltage of VSI at reference value of V_{dcref}. However, instantaneous voltage across C_{dc} is denoted as v in following text.

3. CONTROL SCHEME OF DYNAMIC VOLTAGE RESTORER (DVR)

The generation of reference voltages for dynamic voltage restorer is given as in equation (1)

$$v^*_{dvr}(abc) = v^*_1(abc) - v_s(abc) \quad (1)$$

$$v^*_{la} = V_m \sin(\omega t)$$

$$v^*_{lb} = V_m \sin\left(\omega t - 2\pi/3\right) \quad (2)$$

$$v^*_{lc} = V_m \sin\left(\omega t + 2\pi/3\right)$$

Where $v_l^*(abc)$ and $v_s(abc)$ are desired load voltages and sag/swell effected supply voltages in three phases. Then these reference injected voltages are compared with measured actual injected voltages and generate the switch commands for VSI by using hysteresis voltage control methods.

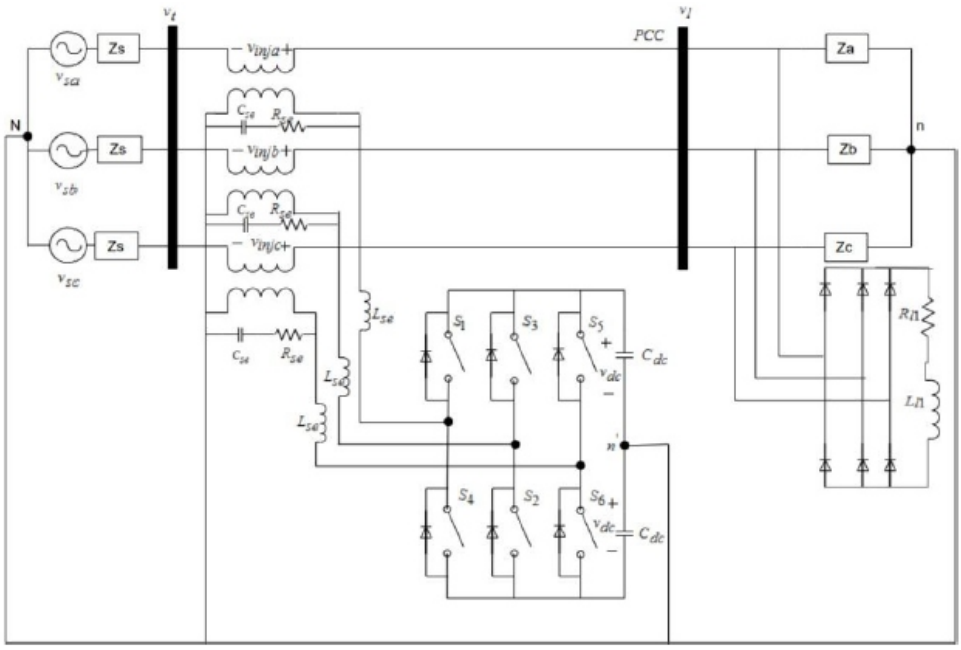


Fig.1. Conventional Three-phase three Leg-Four Wire DVR topology

3.1 Switching band control of the DVR

The reference voltage v_{ref} for the DVR are calculated using a suitable reference calculation algorithm. This reference voltage synthesized by a VSI is injected to the line shown in Fig.2. Appropriate switching pulses for the VSI are generated using switching band controller. With a hysteresis band h about the reference voltage, the lower and upper boundaries $v_{ref} - h$and $v_{ref} + h$are defined. The inverter output voltage is made to track the reference within this band. When the DVR voltage V_{DVR} goes below the lower boundary, a positive dc voltage is applied across the ac filter capacitor by turning ON S_1. If it exceeds the upper boundary, negative voltage is applied through S_4. The control logic thus given as,

$$if\ v_{dvra} \geq v^*_{refa} + h, S_1 = 0, S'_4 = 1 \text{(top switch is ON, bottom switch is OFF)}$$

$$elseif\ v_{dvra} \leq v^*_{refa} - h, S_1 = 1, S'_4 = 0 \text{ (top switch is OFF, bottom switch is ON)} \quad (3)$$

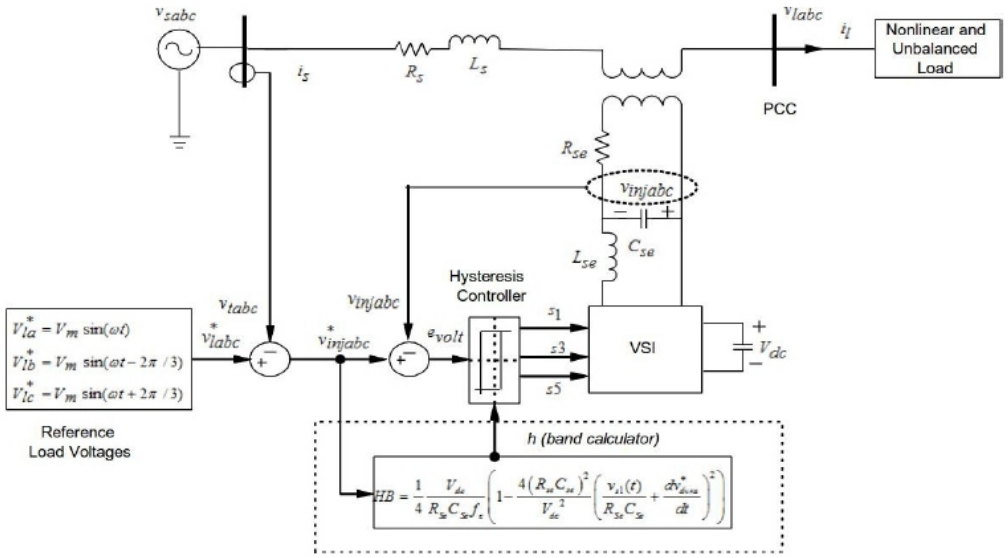


Fig.2. Block diagram of reference injected voltage generation and hysteresis controller

The switching pulses for the other legs of VSI can also be generated following the same logic and using the reference voltages in that particular leg. In the DVR compensator system, the transformer inductance L_{se} with filter capacitor C_{se} forms a filter shown in Fig.3 (a). Here inductance L_{se} is the sum of the leakage inductance of the injection transformer and series interface inductance, i_{inv} is the inverter output current, i_{load} is load current and is the capacitor branch current. v_{inv} is inverter output voltage whose polarity will depend upon the switching signal obtained by hysteresis controller. The LC combination leads to a second order characteristic equation and hence the DVR voltage trajectory is second order response between the two boundaries. The parabolic trajectory can be attributing in this nature. Due to these oscillations over the capacitor voltage, when it reaches upper or lower boundary, a linear return is not ensured even though a reverse dc voltage is applied using control algorithm [9]. This may lead to a frequent violation, results in poor quality of load voltages with increased THD as shown in Fig. 3 (b). Further, the capacitive impedance at switching frequency is lesser, leading to a higher value of capacitor current. Since the VSI rating is independent of the filter current, the cost of DVR is increased. The above drawbacks of the conventional filter are overcome by the proposed filter structure described in the following sub-section.

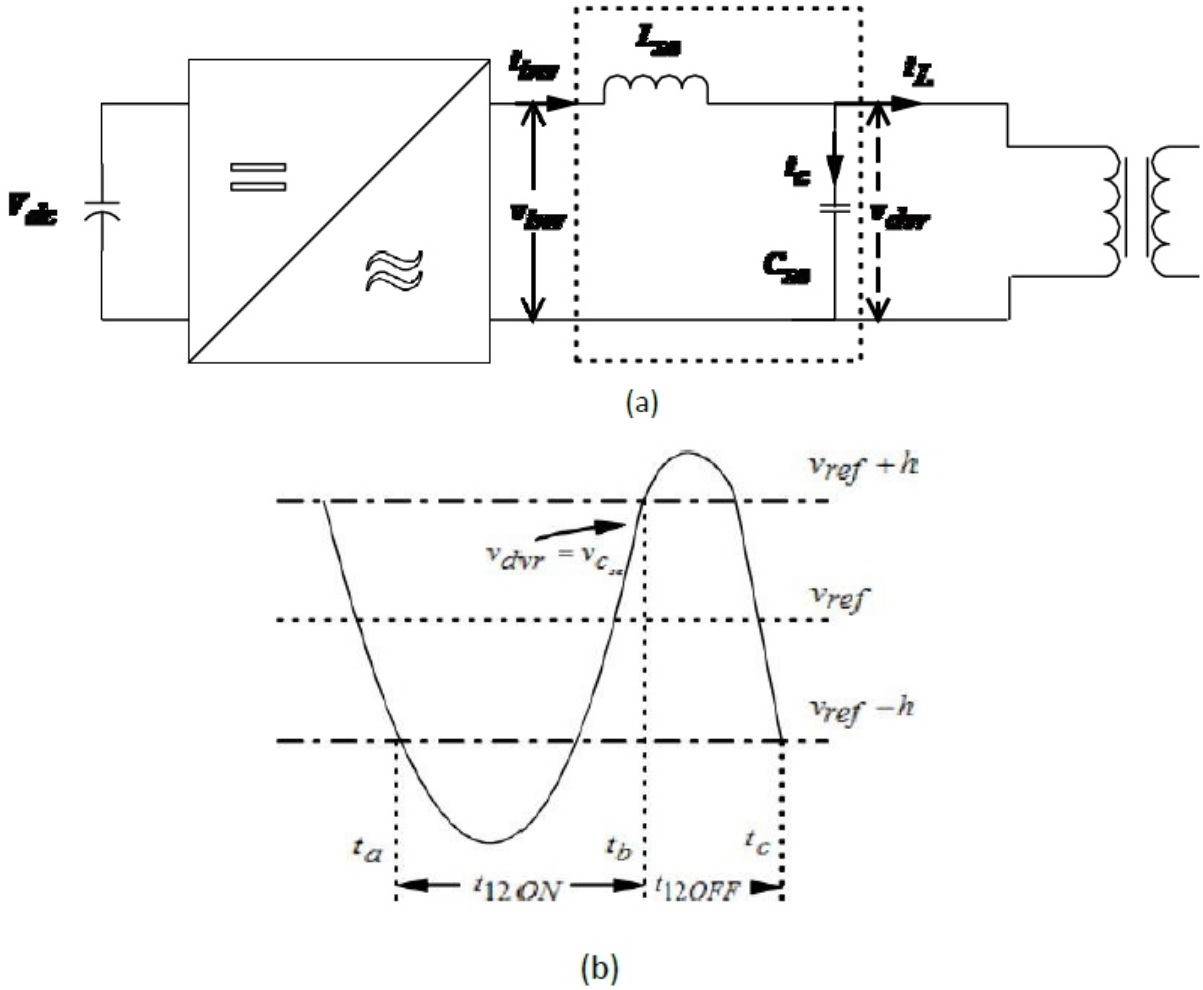


Fig.3 (a) Conventional DVR filter circuit, (b) Conventional DVR filter circuit tracking responseto band controller.

3.2 A modified filter structure for band controller

In order to improve the controller performance, a resistor is added in series with filter capacitor as shown in Fig.4 (a).This resistor presented as a switching band resistor (R_{se}). This resistance dominates

the capacitive reactance at switching frequency, makes the resistive voltage drop v_{Rsw} more than the capacitive reactance voltage drop ( ). The filter acts like R-L circuit at this frequency, making the current in the resistor linear as shown in Fig.4 (b). Here the voltage across the capacitor-resistor pair is called as DVR voltage (v_{dvr}), which is injected external to the DVR. Because of DVR voltage is linearly varying within the boundary, the band controller works like a first order system and the DVR voltage is always within the boundary. Moreover, the presence of more impedance contributed by resistance at a higher frequency, switching frequency capacitor branch current is limited. Even though this band resistor slightly increases loss, improvement in the band controller performance is quite large.

3.3 Selection of Hysteresis Band (HB)

In this section proposes the selection of the hysteresis band (h) value, in fixed hysteresis band controller the h value is 10% of the compensated current, but it has the disadvantages of the uncontrollable high switching frequency. This high frequency produces a great stress on the power transistor and induces important switching losses. The modified switching hysteresis band

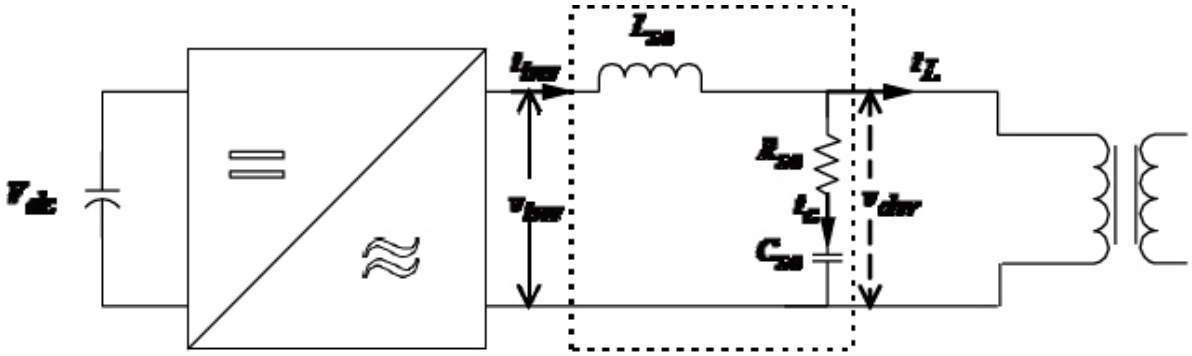


Fig.4 (a) Modified DVR filter circuit for band controller

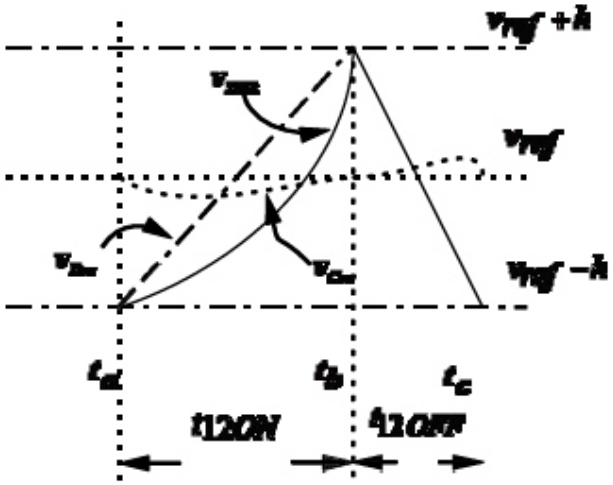


Fig.4(b) Modified DVR filter circuit tracking response to band controller.

3.4 Selection of Hysteresis Band (HB)

In this section proposes the selection of the hysteresis band (h) value, in fixed hysteresis band controller the h value is 10% of the compensated current, but it has the disadvantages of the uncontrollable high switching frequency. This high frequency produces a great stress on the power transistor and induces important switching losses. The modified switching hysteresis band Controller method, the selection of h value depends on the system parameters. Hence this h value allows operation at the nearly constant switching frequency and reduces stress on the power transistor and switching losses. The DVR

modified filter band controller system has been applying KVL and KCL has given circuit as shown in Fig.4.

$$\frac{dv_{dvr}}{dt} = \frac{1}{C_{se}}(I_{inv} - I_L) \quad (4)$$

Where v_{dvr} is the inverter-side voltage and to have paid attention to Fig.5 , the relations can be obtained.

$$v_{dvr} = -v_{inv} + L_{se} C_{se} \frac{dv_{dvr}^2}{dt} + R_{se} C_{se} \frac{dv_{dvr}}{dt} - L_{se}\left(\frac{di_L}{dt}\right) - R_{se} i_L \quad (5)$$

From the geometry of Fig.6, the following equations can be written in the hysterersis-band curvature with respective switching intervals

$$\frac{dv_{dvra}^{+}}{dt} t_{12ON} - \frac{dv_{dvra}^{*}}{dt} t_{12ON} = 2HB \quad (6)$$

$$\frac{dv_{dvra}^{-}}{dt} t_{12OFF} - \frac{dv_{dvra}}{dt} t_{12OFF} = -2HB \quad (7)$$

$$t_{12ON} + t_{12OFF} = T_{sw} = \frac{1}{f_{sw}} \quad (8)$$

Where t_{12ON} and t_{12OFF} are the respective switching intervals, and f_{sw} is the switching frequency.

$$HB = \frac{1}{4R_{se}C_{se}}\left(\frac{V_{dc}}{1} + \frac{4(R_{se}C_{se})^2}{V_{dc}}\left(\frac{v_L(t)}{R_{se}C_{se}} + \frac{dv_{dvra}^{*}}{dt}\right)^2\right) \quad (9)$$

Here, V_{dc} is the dc-link capacitor voltage, dv^*_{dvra} dt is the slope of the reference voltages signals.

The hystersis band HB can be modulated at different points of fundamental frequency to control the switching pluses of the inveter. The calculaed hysteresis bandwidth HB is applied to the switching operation of hystersis controller.

4. SIMULATION STUDIES

The load voltage regulation with three-phase four-wire DVR topology as shown in Fig. 2 is realized by simulation in MATLAB. The load and DVR system are connected at the PCC. The ac load consists of a three-phase unbalanced load and three-phase diode bridge rectifier feeding a highly inductive R-L load.The system and DVR parameters are given in table 1.

Table 1 System Parameters for Simulation Studies

System quantities	Values
System voltages	V_m = 200 V peak voltage, 50 Hz
Feeder impedance	$Zs = 1+j3.14\Omega$
Non linear load	Three-Phase bridge rectifier consisting of R-L Load (100Ω and 10mH)
Linear load	Unbalanced load: Z_{la}=50+j31.41Ω, Z_{lb}=75+j31.41Ω, Z_{lc}=150+j3.141Ω
VSI parameters	R_{se} =1Ω, C_{se} =30 μF and L_{se} = 5mH
Coupling transformer	10MVA,200/200,50Hz, R=0.002 pu, X=0.6 pu
DC link voltages	V_{dcref}=1100 V, C_{DC1} =2,200μF and C_{DC2} =2,200μF
Hysteresis band	h =± 7

The reference voltages are generated using Eqns 1 to 2, and these reference voltages are compared to the actual injected voltages using hysterisis band control. The switching pulses are generated through band controller and in this section switching frequency is improved by using modified filter structure for band controller.

4.1.1 Considering With fixed h value

In this case it is assumed steady state condition the simulation time is taken as t = 0 s to t = 0.08 s with constant nonlinear load and unbalanced load. Voltage sag of a 44% without phase jump was considered in all phases of the source voltages. The voltage sag occurs at time t = 0.02 s and is cleared at time t = 0.04 s, consequently the load voltages attain nominal voltage. The supply voltages and load voltages are plotted in Fig.5 (a).The load voltages have THDs of 4.9% respectively. To regulate load voltages with help of DVR system using improved filter structure band controller with fixed h = ± 7(considering 10% of compensated current). Initially before compensation to generate the accurate reference voltages (V) by using equation (1) are plotted Fig. 5(b).

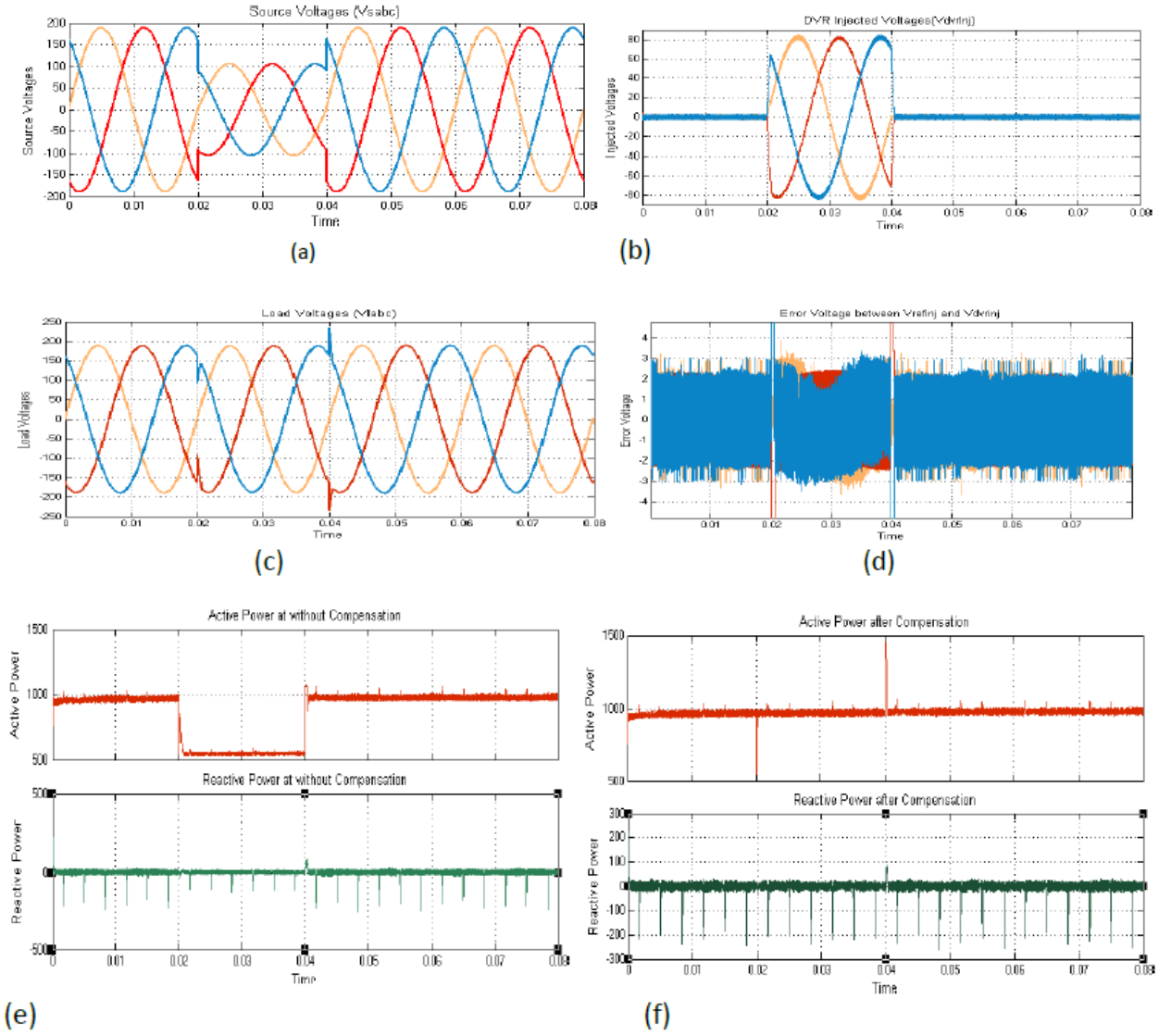
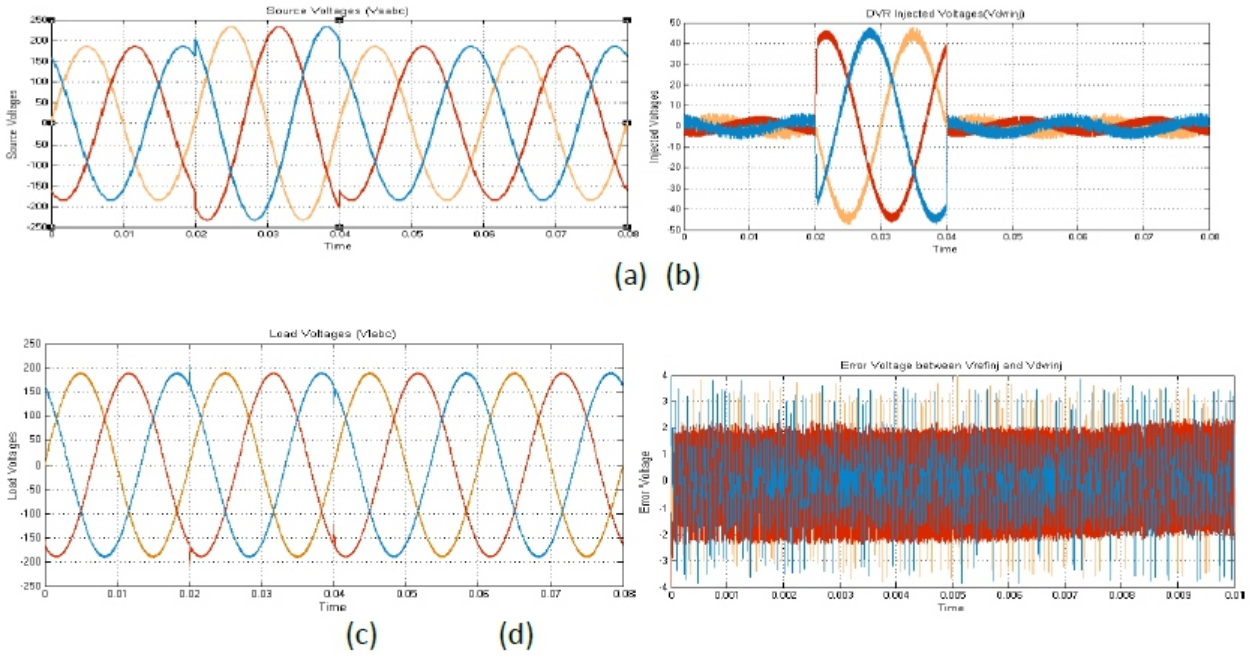


Fig.5 (a) Source voltages (Vsabc),(b) Injected voltages (Vdvrinj), (c) Load voltages (Vlabc), (d) Error between reference injected voltages and actual injected voltages (e) active and reactive power without compensation and (f) active and reactive power after compensation

The Instantaneous DVR injected voltages (V_{dvrinj}) is compared with reference DVR voltages (V) with fixed hysteresis band (h=±6.9) value. At this point when the sensed output signal strays from the reference by more than a prescribed value, the inverter is worked to diminish the deviation. Hence the VSC injected the accurate injected voltages with minimum phase jump angle, and compensate load voltages becomes pure sinusoidal is shown Fig. 5(c) with 0.77% total harmonic distortions. After compensation active power also compensated during the sag intervals of time is shown in Fig. 5(c). The main drawback of the fixed hysteresis voltage Controller is output current having small ripples due to constant hysteresis band, switching losses at converter are more and error between reference DVR voltages (V) and The Instantaneous DVR injected voltages (V_{dvrinj}) are more is shown Fig. 5(d), now to reduce these drawbacks with help of adaptive Hysteresis voltage controller. Finally, the DVR Injects active power during sag interval of time and maintain constant active power are shown in Fig 5(e) and 5(f).

4.1.2 Considering with Variable Hysteresis Band (HB)

In case 2 applied a 25% of the swell was considered in all phases of the terminal at the time of interval 0.02s to 0.04s and applied adaptive hysteresis voltage controller. In adaptive hysteresis voltage controller, the HB value can calculate at the nearly constant switching frequency and is usually performed by software which uses the system parameters by using equation (9). The modified The Instantaneous DVR injected voltages (V_{inj}) is compared with reference DVR voltages (V) at instantaneous hysteresis band (HB) with each sample time and constant switching frequency (fc) technique. The modified Instantaneous DVR injected voltages (V_{dvrinj}) are shown Fig. 6(b) and hence load voltages become pure sinusoidal without ripples shown in Fig. 6(c) with 0.27% total harmonic distortions. Finally, by using adaptive hysteresis band voltage controller to Error between reference currents (V_{ref})and Instantaneous injected currents (V_{inj}) are very less shown Fig. 6(d) and active power and reactive power compensations are shown in Fig.6(e) and 6(f)



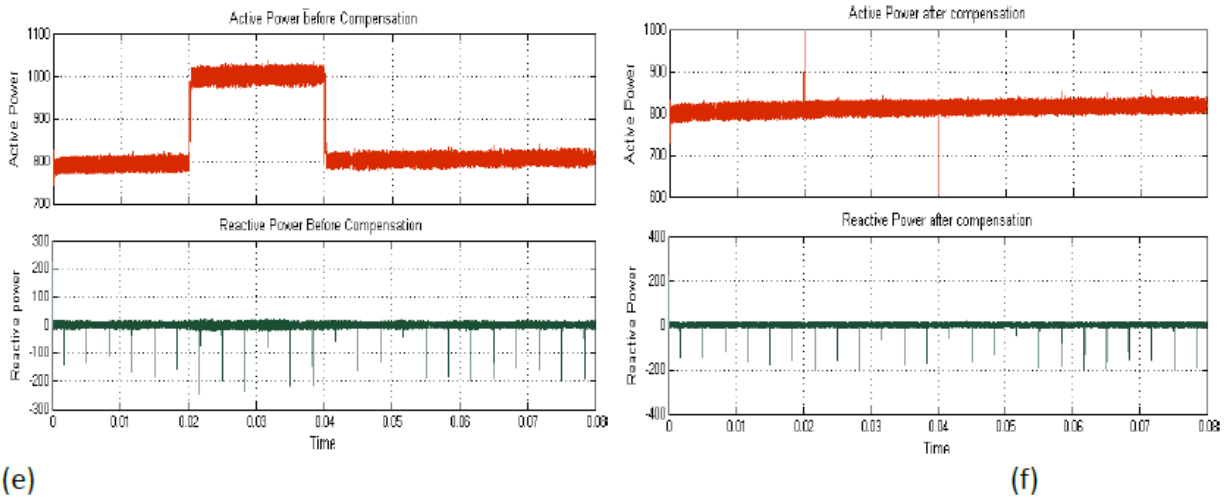


Figure 6 (a) Source voltages (V_{sabc}),(b) Injected voltages (V_{dvrinj}), (c) Load voltages (V_{labc}), (d) Error between reference injected voltages and actual injected voltages (e) Active and reactive power before compensation and (f) Active and reactive power after compensation.

4.1.3 Mitigation of Voltage Harmonics at PC

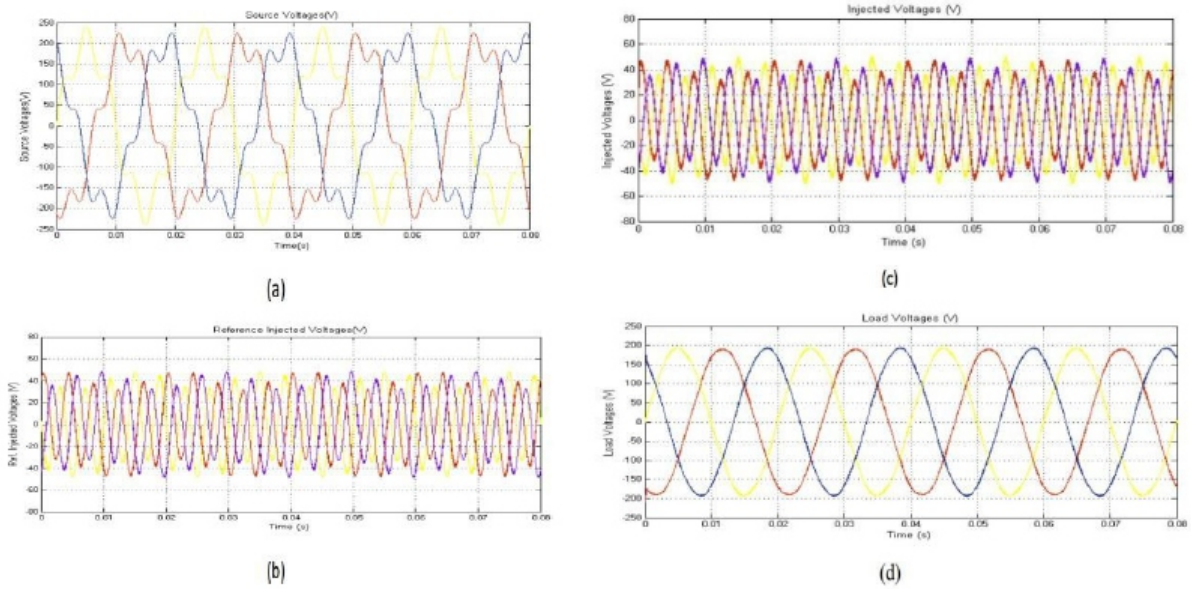


Fig.7 (a) Source voltages (V_{sabc}), (b) Reference Injected voltages (V_{refinj}), Injected voltages (V_{dvrinj}), and (d) Load voltages (V_{labc}) with compensation.

In this case it assumed that the source voltages contains the fifth-order harmonic with a value of 20% amplitude in the interval 0s to 0.08

TABLE 2. THD% OF PCC Voltages

Load Voltages	THD (%)	
	Without compensation	With compensation
V_{ta}	20.01	1.346
V_{tb}	20.01	1.283
V_{tc}	20.01	1.178

5. CONCLUSION

A VSI topology for DVR regulating the load voltages under different voltage related problems are presented. The modelling of modified filter circuit band controller is discussed for carrying out the simulation studies and reduced switching losses and maintains constant switching frequency. Variable hysteresis band controller generates accurate injected voltages with help of system parameters and having low error value between reference injected voltages and actual injected voltages, smooth and no ripples in voltages.

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Real Time Object Tracking in Surveillance System using MATLAB

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ABSTRACT

In video surveillance, detection of moving objects from a video is important for object detection, target tracking, and behavior understanding. Detection of moving objects in video streams is the first relevant step of information and background subtraction is a very popular approach for foreground segmentation.. Nowadays CCTVs are installed at many places like banks safe. But the CCTV cameras continuously record the situations. Hence there is an unnecessary memory wastage if there is nothing happening in front of the camera. Also the CCTV system does not provide alerts of burglary happening at particular time. So there is a need of a system which will record the situation only if there is some movement happening in front of the camera.. By implementing the system in real time and testing the system on large number of long sequences, authenticated person can stop alert for fix time to enter into secured. Human motion Detection System is developed from the security point of view. The objective of Real Time Security System using Human Motion Detection is to develop a system that monitors the area in which it is being deployed. In Human motion detection System, web camera is applicable in the area where no one is permissible to enter, also where we need to detect if any motion has been done. We can use web camera for Human Motion Detection. The Camera is used to catch the live images of the area in which it is being implemented, if any object is moving. The captured images are stored for further work. The captured images are stored for further work. If motion is found in this video, the computer will start recording, buzz an alarm.

Keywords: Object detection, Background subtraction, Gaussian Mixture model, Real Time Video, Surveillance Camera.

INTRODUCTION

Surveillance cameras can be an effective technique to protect public safety and detect or deter criminal activity. Surveillance cameras are increasingly being installed inside and outside of public buildings (in elevators, hallways, entrances, etc.), on streets, home, highways, in parks and public transportation vehicles. Carlos and Fernando gives an automatic visual object detection and tracking framework is proposed to reliably introduce video surveillance and counting-based applications in the consumer electronics environment. It is based on off-the shelf equipment, such as IP, web cameras, and PCs, and does not need especial installation and configuration requirements [1]. The video surveillance system requires fast, reliable and robust algorithms for moving object detection and tracking. The system can process both colour and gray images from a stationary camera. It can handle object detection in indoor or outdoor environment and under changing illumination conditions [2] Habib Hussien presented a live feed frames sequences from a fixed camera, detecting all the foreground objects and estimate the trajectory of the object of interest moving in the scene. There are many challenges in developing a good object detection algorithm [4]. The video captured by the camera is being processed by the MATLAB

program that helps in motion detection. [2] Frame difference used in this paper, which calculates the differences between 2 frames at every pixel position and store the absolute difference. It is used to visualize the moving objects in a sequence of frames.

Generalized system

Existing system was simply based on frames or we can say objects. Simple approach was used in existing system like capturing photos or frames with CCTV camera. After capturing frame it will calculate the difference between captured frames[8].Then it will calculate the threshold value by applying some algorithmic standards and it will detect the objects based on the motion of that object

Fig -1: Block Diagram

a-Moving Object Detection

Moving object detection is always the first step of a typical surveillance system. Moving object detection aims at extracting moving objects that are interesting out of a background which can be static or dynamic. Since subsequent processes are greatly dependent on the performance of this stage, it is important that the classified foreground pixels accurately correspond to the moving objects of interests. The three most popular approaches to moving object detection are background subtraction, frame differencing, and optical flow.

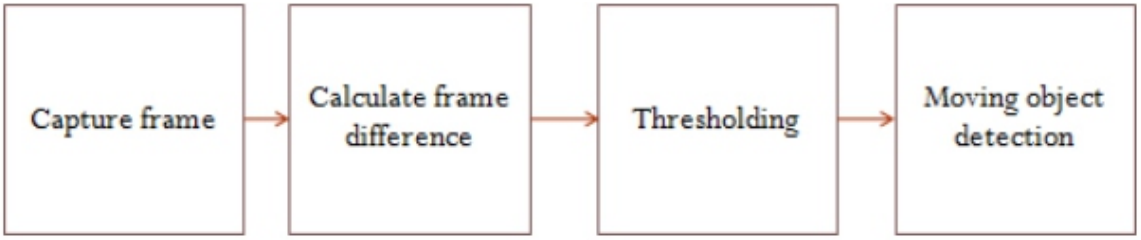

Fig -2: Traditional object detection

b-Object Tracking

Object tracking is to establish a correspondence between objects or object parts in consecutive frames and to extract temporal information about objects such as trajectory, posture, speed and direction. Tracking detected objects frame by frame in video is a significant and difficult task. It is a crucial part of smart surveillance systems since without object tracking, the system could not extract cohesive

temporal information about objects and higher level behavior analysis steps would not be possible. On the other hand, inaccurate foreground object segmentation due to shadows, reflectance and occlusions makes tracking a difficult research problem. Object Tracking in real-time objects is done on the basis of the environment properties of the object such as Bounding Area, Centroid etc.

c-Moving a Object Tracking Based On Region

This method identifies and tracks a blob token or a bounding box, which are calculated for connected components of moving objects in 2D space. The method relies on properties of these blobs such as size, color, shape, velocity, or Centroid. A benefit of this method is that it time efficient, and it works well for small numbers of moving objects. Partial overlapping and occlusion is corrected by defining a pedestrian model. From the above Object tracking system flow chart, we can see that we apply morphological filters based on combinations of dilation and erosion to reduce the influence of noise, followed by a connected component analysis for labeling each moving object region.

PROPOSED METHODOLOGY

a- Foreground Detection

A combination of a background model and low-level image post-processing methods to create a foreground pixel map and extract object features at every video frame. Background models generally have two distinct stages in their process: initialization and update.

b- Gaussian mixture Model

A Gaussian Mixture Model (GMM) is a parametric probability density function represented as a weighted sum of Gaussian component densities. GMMs are commonly used as a parametric model of the probability distribution of continuous measurements or features in a biometric system, such as vocal-tract related spectral features in a speaker recognition system. GMM parameters are estimated from training data using the iterative Expectation-Maximization (EM) algorithm or Maximum A Posteriori (MAP) estimation from a well-trained prior model.

Main Body Text :A novel adaptive online background mixture model that can robustly deal with lighting changes, repetitive motions, clutter, introducing or removing objects from the scene and slowly moving objects. Their motivation was that a unimodal background model could not handle image acquisition noise, light change and multiple surfaces for a particular pixel at the same time. Thus, they used a mixture of Gaussian distributions to represent each pixel in the model.

To implement an 8 mixture of Gaussians. But the pixel values that don't fit the background distributions are considered as foreground. Nowak 2003 showed how the parameters of a mixture of Gaussians for which each node of a sensor network had different mixing coefficients could be estimated using a distributed version of the well-known expectation-maximization (EM) algorithm. This message-passing algorithm involves the transmission of sufficient statistics between neighboring nodes in a specific order, and was experimentally shown to converge to the same results as centralized EM. Kowalczyk and Vlas-sis Kowalczyk and Vlassis, 2004 proposed a related gossip- based distributed algorithm called Newscast EM for estimating the parameters of a Gaussian mixture. Random pairs of nodes repeatedly exchange their parameter estimates and combine them by weighted averaging.

In this section, another technique that is commonly used for performing background segmentation. Stauffer and Grimson et al. have proposed; suggest a probabilistic approach using a mixture of Gaussian for identifying the background and foreground objects. The probability of observing a given pixel value Ptat time t is given by

$$P(p_t) = \sum_{i=1}^{k} \omega_{i,t}\, \eta(p_{t,i}\, \mu, \sum i,t)$$

$$P(p_t) = \sum_{i=1}^{k} \omega_{i,t}\, \eta(p_{t,i}\, \mu, \sum i,t)$$

Where k is the number of Gaussian Mixture and that is used. The number of k varies depending on the memory allocated for simulations. Then the normalized Gaussian η is a function of ωi,tμi,t Σi, t which represents weight, mean and co-variance matrix of the ith Gaussian at time Where k is the number of Gaussian Mixture and that is used. The number of k varies depending on the memory allocated for simulations. Then the normalized Gaussian η is a function of ωi, tμi, t Σi, t which represents weight, mean and co-variance matrix of the ith Gaussian at time

$$\rho = \alpha\eta(\ p_t |\ \mu_{i,t-1},\ \sigma_{i,t-1})$$

$$\omega_{i,t} = (1-\alpha)\omega_{i,t-1} + \alpha$$

$$\mu_{i,t} = (1-\rho)\mu_{t-1} + p_t\rho$$

$$\sigma^2_{i,t} = (1-\rho)\mu_{t-1} + p_t\rho$$

The values for weight and variance vary based on the significance that is given toa pixel which is least likely to occur in a particular way. All the Gaussian weights are normalized after the update is performed. The-Gaussians are then reordered based on their likelihood of existence.

C - Background Subtraction Detection

Background subtraction method initializes a reference background with the first few frames of video input. Then it subtracts the intensity value of each pixel in the current image from the corresponding value in the reference background image. The difference is filtered with an adaptive threshold per pixel to account for frequently changing noisy pixels. The reference background image and the threshold values are updated with an IIR filter to adapt to dynamic scene changes. Background subtraction (aka background differencing) is probably the most fundamental image processing operation for video security applications. Frame differencing is a pixel-wise differencing between two or three consecutive frames in an image sequence to detect regions corresponding to moving object such as human and vehicles. The threshold functions determine change and it depends on the speed of object motion. It's hard to maintain the quality of segmentation, if the speed of the object changes significantly. Frame differencing is very adaptive to dynamic environments, but very often holes are developed inside moving entities. Videos are actually consists of sequences of images, each of which called as a frame. For detecting moving objects in video surveillance system, use of frame difference technique from the difference between the current frame and a reference frame called as 'background image' is shown.

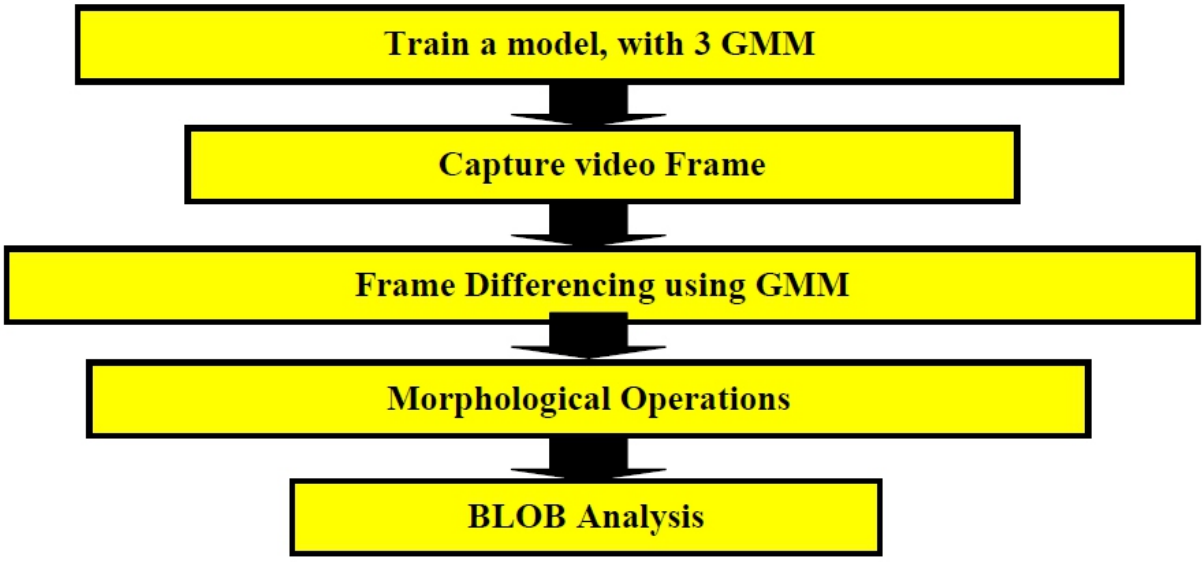

Fig -3: Flowchart for Background Subtraction

Algorithm for person alert

Step 1: Capture frame from camera in real time.
Step2: Convert the RGB image to Gray scale.
Step3: Get the current and the last frames.
Step4: Find the difference between these two frames.
Step5: Threshold this image.
Step6: Check if the difference value between the two frames (i.e. rate of movement) is greater than the value set by the user.
Step7: If yes buzz the alarm. Detection Algorithm

Input: Frame f captured at time t and Frame f captured at time t+1, Th as Threshold
Output: Alarm

Process:
1. Convert frames into grayscale
2. Calculate difference of Frames.

$$D(x,y,t+1)=\begin{cases}1 & |f(x,y,t)-f(x,y,t+1)>Th| \\ 0 & otherwise\end{cases}$$

3. Th for decision to set foreground and background pixel
4. Get binarized image
5. Get moving object
6. If moving object motion>threshold2 then send Alert Alarm

APPLICATIONS

The name of this topic itself is one of the applications of the system. The term surveillance is a most applicable to security system because in the security system, to watch on every suspicious movement in the specific organisation. The advances in the development of these algorithms would lead to

breakthroughs in applications that use visual surveillance. Monitoring of Banks, Departmental Stores, Airports, Museums, stations, private properties and parking lots for crime prevention and detection patrolling of highways and railways for accident detection, Measuring traffic flow. In such organisation this system is most not only applicable but also more reliable. The demand for remote monitoring for safety and security purposes has received particular attention, especially in the following areas: Transport applications such as airports, auditorium environments, railways, and motorways to survey traffic.

Public places such as banks, supermarkets, homes, department stores and parking lots. Remote surveillance of human activities such as attendance at football matches or other activities. Surveillance to obtain certain quality control in many industrial processes, surveillance in forensic applications and remote surveillance in military applications.

CONCLUSIONS AND RESULTS

A video monitoring detecting system was thus developed successfully in this project. This system mainly provides an efficient method for surveillance purposes and is aimed to be highly beneficial for any person or organization. Thus motion based change detection in.avi video format was completed and successfully implemented. We propose an instance based method for human detection in real time, which is motivated by a range of applications. An implementation and system design of a prototype system developed for testing purposes is reviewed in this report as well. In this report, a human body detection algorithm based on the combination of temporal information and shape information is designed. Firstly, the area are selected which are surveillance. Where the need of object are detected. When the moving object is entering in the surveillance area it will be detected. Moving objects are detected using the proposed Background Elimination Technique and Gaussian mixture Model. Secondly, the moving a object are track under the surveillance area and the .outside rectangle of moving object is computed using the max width and height value of the moving regions.

Fig -4: Area under Surveillance

Fig -5: Track Object Image

Fig -6: Object Detected

Fig-7: Background Eliminated Frame

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