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Journal of Electrical Engineering and Advanced Technology

Aims and Scope

Journal of Electrical Engineering and Advanced Technology is a journal that publishes original research papers in the fields of Electrical Engineering and Advanced Technology and in related disciplines. Areas included (but not limited to) are electronics and communications engineering, electric energy, automation, control and instrumentation, computer and information technology, and the electrical engineering aspects of building services and aerospace engineering, Journal publishes research articles and reviews within the whole field of electrical and electronic engineering, new teaching methods, curriculum design, assessment, validation and the impact of new technologies and it will continue to provide information on the latest trends and developments in this ever-expanding subject.

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Contents

Design and Implementation of Low Power High Speed 4*4 Bit Multiplier using Vedic Mathematics

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ABSTRACT

Multiplier plays an significant role in electronic circuits. In many apps, such as digital signal handling, microprocessors and micro commuters, these are the primary blocks. In this document we propose a high-speed Vedic multiplier pipeline, which contains Vedic mathematics as an old method with a distinctive method and a distinct sutra. This article discusses Sutra Urdhva Triyagbhyam (UT), which is effective in terms of the multiplier's field and velocity. We have introduced distinct architectures to increase the velocity of the multiplier, where the complete addition from distinct logics is used. The Vedic multiplier in this document is intended with a modified full-adder that uses less slices and delay is reduced. The model is simulated using Xilinx 14.7 version and synthesized using RTL compiler.

Keyword - Vedic Multiplier, Full Adder using Multiplexer, Ripple Carry Adder.

I. INTRODUCTION

Multiplier is one of the main hardware blocks for arithmetic, signal and picture treatment design. Multiplier with improvements in technology, many scientists have attempted to design multipliers with high velocity, low energy regularity, regularity of layout, and therefore less area or even the mixture of them into a multiplier. In addition, many transformer algorithms such as Fast Fourier (FFTs), DFT, etc. Digital Signal Processors are speeded for the multiplier. Urdhva Tiryakbhyam Formula is conducted using two cross-sectional and diagonal multiplication methods. Then their amount will lastly be taken.

High-speed multipliers play an significant role during architecture design in latest years, while scientists continue to work on many variables to improve the machining velocity of these fundamental components. The complexity of multiple apps reduced, requiring both quicker multiplier chips and perceptual and effective chip multiplier algorithms. The Vedic propagation is based on the Vedic formulae. These formulas have traditionally been used in the decimal number system to multiply two numbers..

II. URDHVA TIRYAKBHYAM SUTRA

Urdhva Tiryakbhyam is a general formula for multiplication relevant to all instances of vertical and cross-technical multiplication. This paper is used to design the digital multiplier architecture for the binary number scheme Urdhva Tiryakbhyam Sutra. Vedic mathematics is used because it reduces to

very easy the typical calculations in popular mathematics. Vedic mathematics is an arithmetical rules methodology which makes it possible to implement velocity more effectively.

Urdhva Tiryakbhyam Sutra is a general formula for multiplication in all instances. It implies "vertically and cross sectionally." The numbers are multiplied on the two ends of the row and the outcome is added to the prior line. If in one step there are more lines, the outcomes will be added to the prior transmission. This means that the least significant digit of the amount is one of the figures, the remainder being the lead for the next phase. The carriage is taken to be zero in the beginning. for the next step. Initially the carry is taken to be as zero.

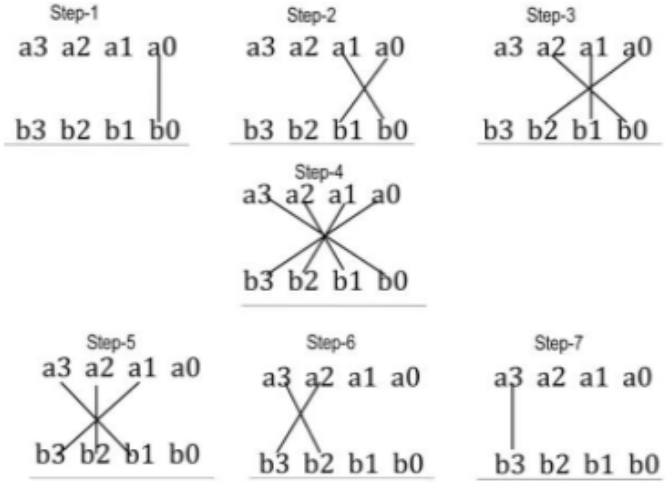

Fig.1: Line diagram for 4*4 multiplication using Urdhva Tiryakbhyam Sutra

In order to illustrate an example, we will consider the vertical multiplication by cross section of two multiplicand binary numbers a3a2a1a0 and two n-bit multipliers b3b2b1b0. The multiplication of two n-bit numbers would result in the product of 2n-bit, each stage of operation can be indicated in a line graph Fig.1. From convention multiplier all partial products are calculated in parallel and shifting of partial product is eliminated in case of Urdhva-Tiryakbhyam sutra and hence it is more efficient.

The above line diagram representation of Vedic multiplier is implemented using equation shown below with operands X and Y.

X=a3a2a1a0 Y=b3b2b1b0

P0=a0b0

P1=a1ab0+a0b1+c1

P2=a2b0+a1b1+a0b2+c2

P3=a3b0+a2b1+a1b2+a0b3+c3

P4=a3b1+a2b2+a1b3+c4

P5=a3b2+a2b3+c5 P6=a3b3+c6

P7=c7

III. PROPOSED VEDIC MULTIPLIER

Here in this design we have changed full adder using multiplexer instead of XOR and OR gate Full Adder.

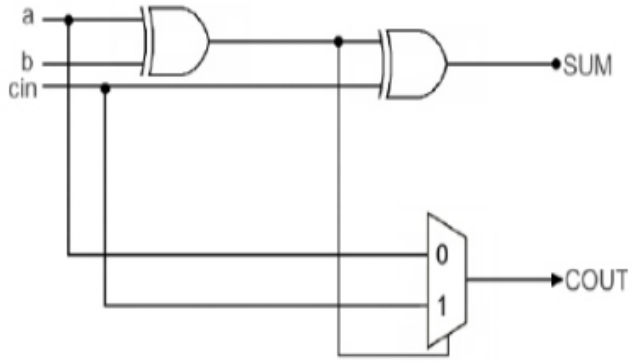

Fig:2 Full adder using 2:1 Multiplexer

Full adder could probably be an important square structure of explicitly integrated circuits for multiple applications. Multiplexer is used to find the entire Full Adder and another is used in order to achieve the complete Adder output. Two select lines are available for each 4X1 MUX that can be used for selecting one source of input. The 1-bit full adder is one of the most critical processor components for determining the performance, which is used for cache or memory access in the ALU, the floating point unit and for address generation. A 1-bit complete adder is used in the current job, which uses a new multiplexer architecture, which is based on two identical 4:1 multiplexer, That needs the complete adder feature of a total of 28 transistors. The fresh adder has low response time, low energy use and decreased transition activity as other low energy supplements, as it uses only two circuit concentrations.

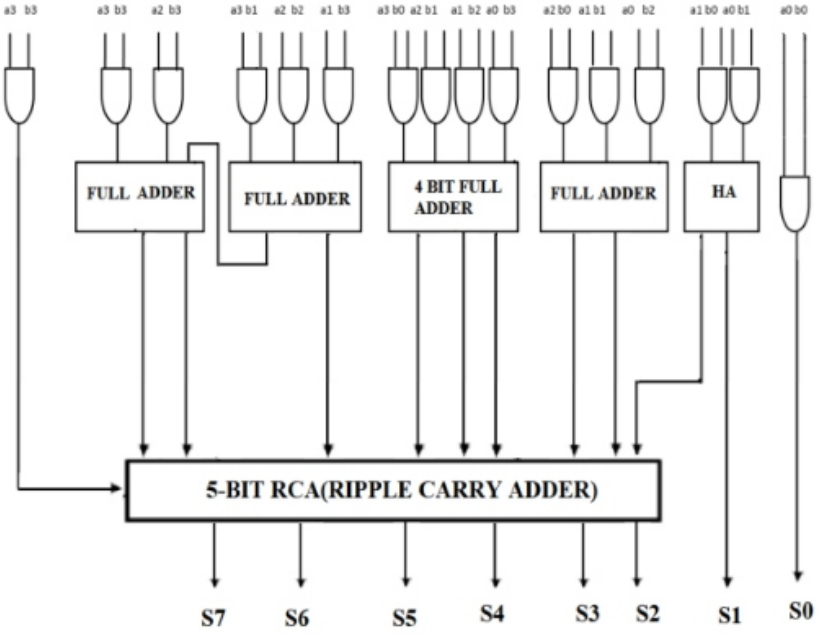

Fig:3 Proposed Vedic Multiplier Using Ripple Carry Adder

The above proposed Vedic multiplier is implemented using equation shown below:

$$S0=a0b0 \quad (1)$$

$$S1=a0b1+b0a0\ldots \quad (2)$$

$$S2=c1+a2b0+a1b1+a0b2. \quad (3)$$

$$S3=c2+a3b0+a2b1+a1b2+a1b3\ldots \quad (4)$$

$$S5=c3+a3b1+a2b2+a1b3\ldots \quad (5)$$

$$S6=c4+a3b2+a2b3\ldots \quad (6)$$

$$S7=c5+a3b3\ldots \quad (7)$$

In 4* 4 Vedic multiplier, it can be understood that the conveyor does not spread to future adders in the early stages as these effects will appear late during the increment. Since the amount of stages increases in velocity, but it causes the overhead area to decrease, less registers are desirable. This reduces the delay in pipeline phases in distinct phases. This suggested main phase model input continues and results are maintained in the first level record while at the same moment other information sources in the first phase are encouraged to level registries.

During the second clock cycle, second-stage data sources are ready and results are registered as second-dimensional, and data sources in the next phase are urged to register in the second dimensions and this operation is carried through to the end. Finally, all additives are treated to swell, transport snake with moving operation and achieve desired results.

IV. SIMULATION RESULT

Simulation and synthesis are done by using Xilinx ISE Suite 14.7 for Spartan-6 family device with a speed grade of -2. In simulation results, Technology View describes top block which shows the set of inputs and outputs. In this proposed Vedic multiplier path delay and number of logic used is less compares to conventional multiplier i.e. 17.213 ns. Register Transfer Logic (RTL) view designates internal architectural blocks along with the connections between input and output pins. Timing waveform is generated by writing test bench program which contains the set of input test vectors applied to design.

V. SIMULATION RESULT OF PROPOSED VEDIC MULTIPLIER

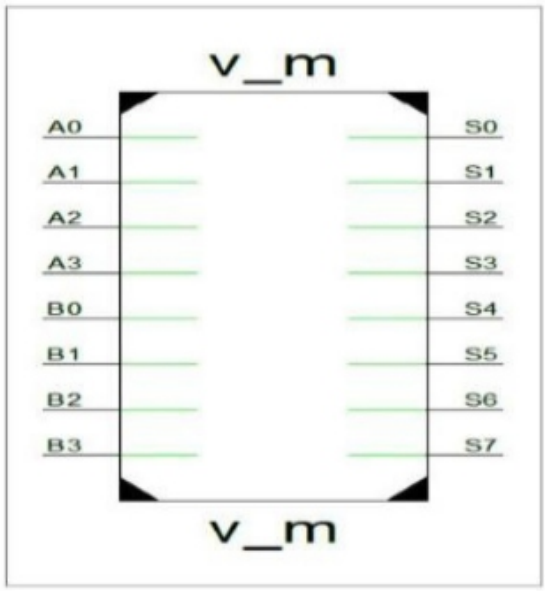

Fig:4 RTL view of Vedic Multiplier

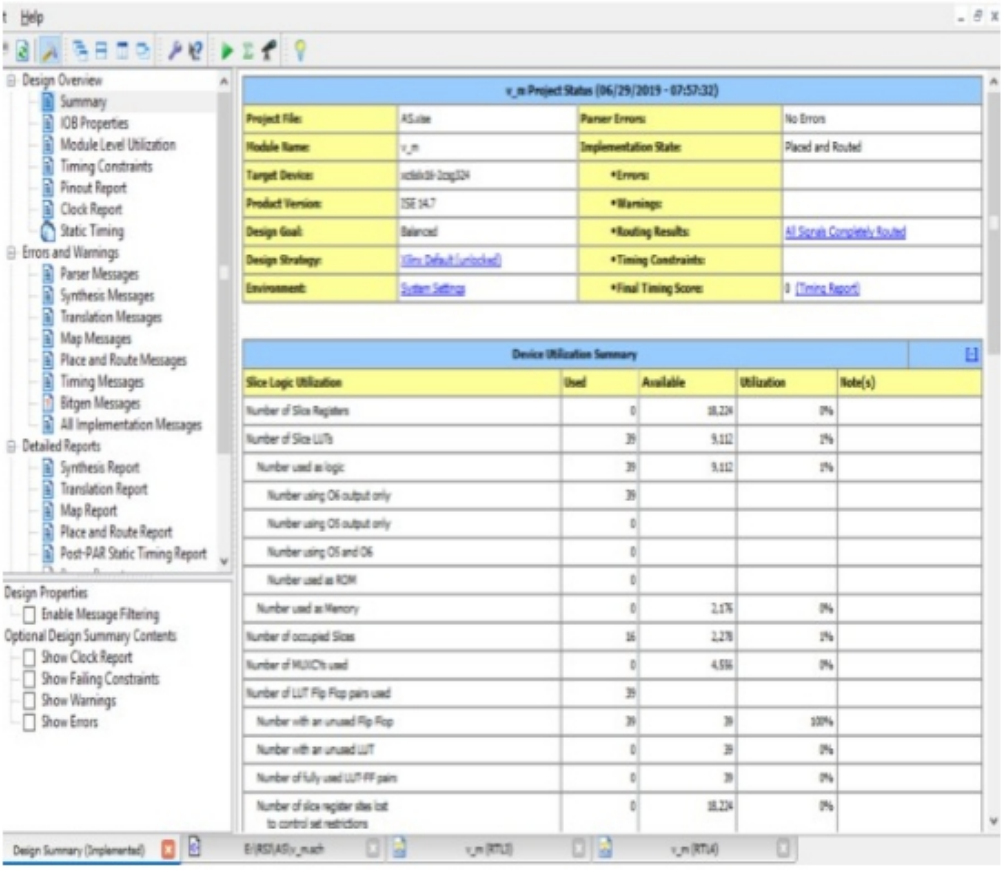

Fig:5 Summary of proposed Vedic Multiplier

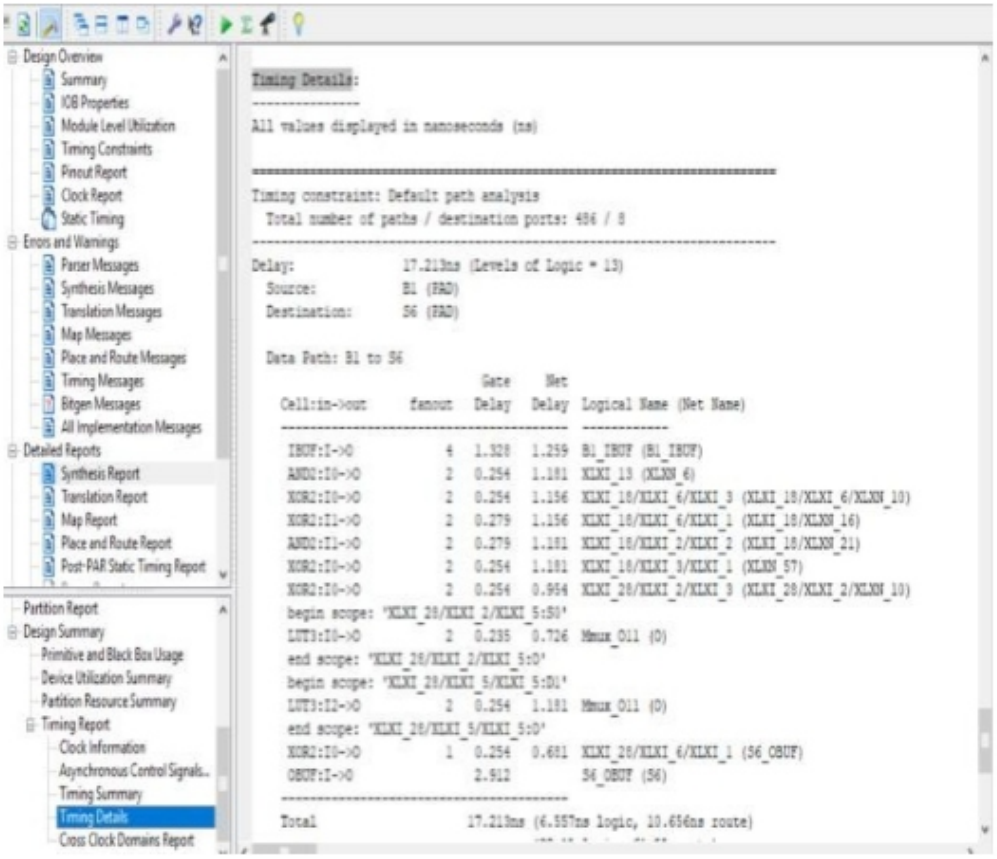

Fig:6 Path delay of proposed Vedic Mutliplier

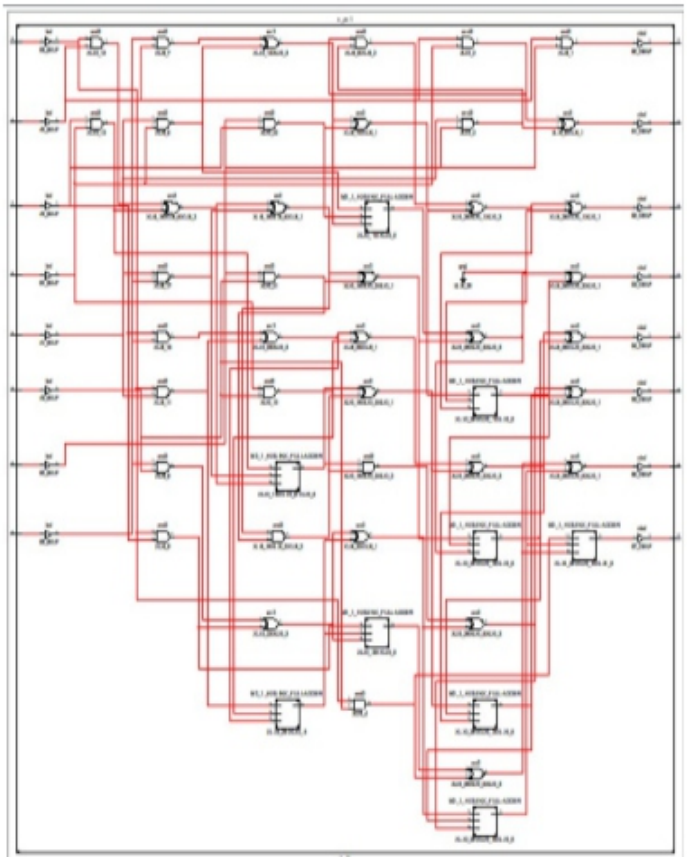

Fig:7 The Technology view of proposed Vedic multiplier

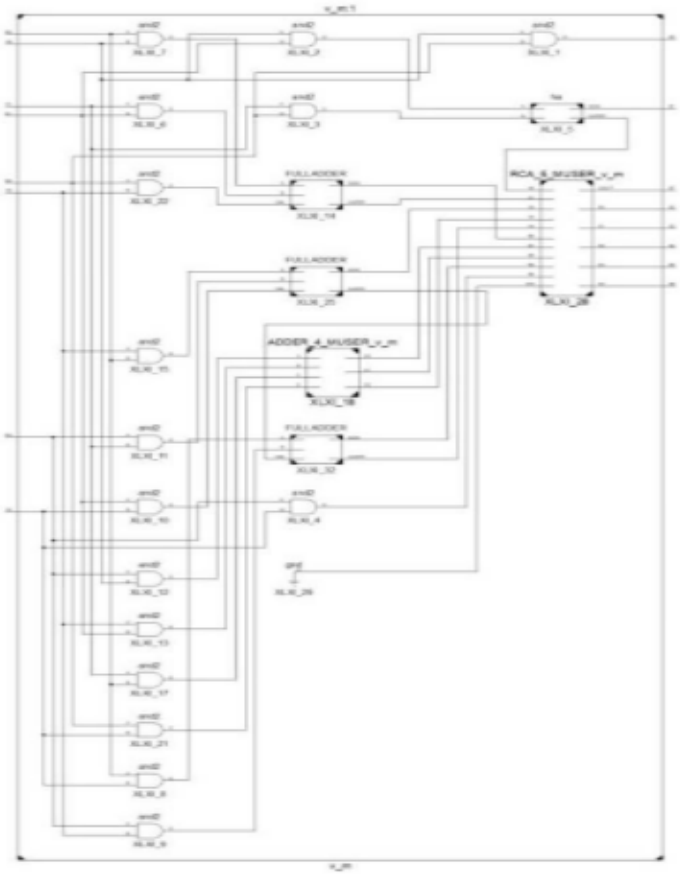

Fig:8 The detailed RTL view of proposed Vedic multiplier

VI. CONCLUSION

We have suggested various methods of Vedic multiplier in this document and also altered complete adder for the construction of 4-bit Vedic multipliers, which leads to a delay and a number of logics in this method.

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Design and Simulation of Vernier Ring Oscillator TDC with Improved Resolution

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ABSTRACT

TDC plays a very important role in most of the in high energy nuclear physics time of flight experiment for achieves high resolution. The traditional time interval experiment measurement totally depend on such kind of methods like Time-to-Amplitude Conversion, Vernier method, Delay Locked Loops (DLL), Tapped Delay Lines (TDL), Differential Delay Lines (DDL), current -Integration TDC, & Counter-Based TDC etc. Many time-of-flight (TOF) applications required measurement of the time intervals between two events. Time to digital converter is becoming more suitable for these kinds of applications because it measures the time difference between two pulses and gives time difference as a digital output code. However, basic TDC needs much higher clock frequency to measure smaller time intervals between two events in terms of picoseconds. The main advantage of migrating TDC in the FPGA paradigm is making the best of its configuration and reconfiguration capabilities. The resolution below the minimum gate delay is achieved by employing Vernier oscillator technique. We present here a high resolution TDC based on vernier ring oscillator principle of nearly 70ps resolution.

Keywords - TOF, Time to Digital Converter, Vernier Delay Line, Field Programmable Gate Array, Ring Oscillator.

I. INTRODUCTION

Time to Digital Converter is widely used in electronic to convert time to digital code. Originally it is developed for nuclear experiments to locate single- shot events; recently, it has been employed to measure phase in all-digital phase-locked loops (PLL) [3]. The TDC is now being used in many applications such as space science instruments, physical instruments, high energy particle detectors phase meters, and digital storage oscilloscopes, laser range finders, and measurement devices. Precise measurements of time interval are performed with the use of various methods in both the analog and digital domains. The digital methods become predominant due to the ease of implementation in integrated circuits, shorter conversion time, and higher immunity to external disturbances. . In all these applications the adoption of the Vernier method permits achieving sub-gate delay time resolution.

First, a physical quantity is converted to a time signal and then digitized by a time-to-digital converter (TDC) to get them corresponding digital output. It measures the time interval between two events. The time intervals between two rising edges or two electrical timing signals, also called start and stop signals, will be quantized and then converted into digital data [2].

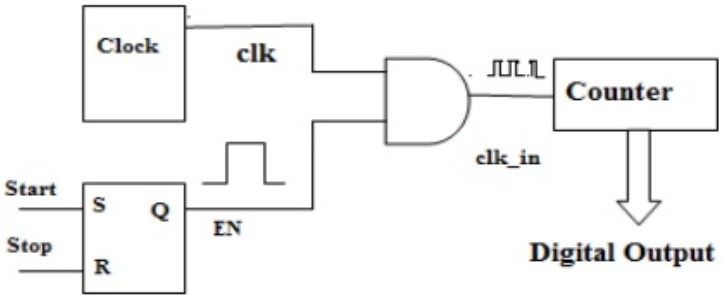

Fig. 1.Basic operation of TDC

A combination of a counter and interpolation has been proposed for a large linear dynamic range and high resolution TDC (Nutt 1968, Kalisz 2004). The counter keeps track of the full clock cycles elapsed since the arrival of the start pulse. The counter is either halted with the stop pulse or the stop pulse stores the state of the counter [2].

II. VERNIER RING OSCILLATOR TDC

The significant blocks of the TDC are ring oscillators, phase detector, and fast counters. The two ring oscillators with a slight difference in the period are obtained as shown in Fig.3. The oscillator design combines features like trigger synchronized starting & stopping and retrigger-ability. The very small and precise difference in periods is achieved by carefully evaluating the place & route delays in both oscillator circuits and by changing the feedback load [7] as shown in Fig.3. In this project, the slow oscillator's And-Or-Invert gate has a fan-in of two and larger delay, whereas the fast oscillator's NOR gate has a fan-in of one and minor delay. This generates a slight difference in periods. Two long duration counters exercised in calibration determines the exact difference in periods and calibrates the TDC.

Here, $T_2 < T_1$ and STOP pulse will come after START pulse, at some point the rising edge of the fast clock will coincide with the rising edge of the slow clock, which will recognize by a phase detector. Circuit for phase detector is given in fig.3

In the FPGA based implementation. There are two oscillators produce signals of frequencies $f\_1 = 1/T$ and $f_2 = 1/T_2$ differing only slightly

The incremental resolution is presented by the difference between T_1 and T_2, given by

$$R = T_{slow} - T_{fast}$$

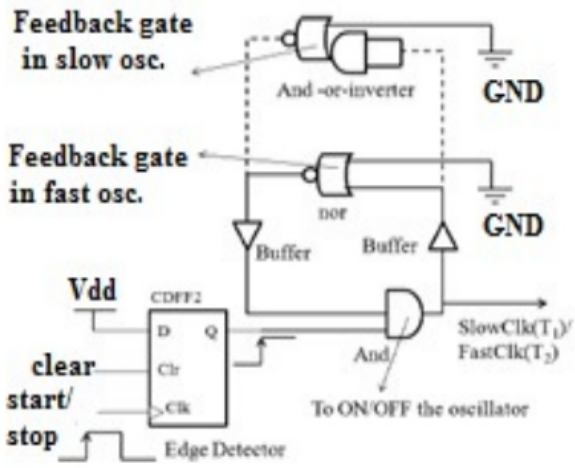

Fig.2. Block diagram of slow & fast Oscillator

The above fig. represents the block diagram of slow and fast oscillator.

III. PROPOSED DESIGN

The proposed design of Vernier Ring Oscillator TDC is the VTDC that utilizes two trigger able oscillators with a precise oscillation frequency difference to replace the VDL in the conventional VTDC. The phase detector keeps track of the history of the phase difference between two oscillators and stops the measurement process once T_1 begins to lead T_2 . On the first rising T_1 edge after the rising edge of T_1, the output of the first register Q_1 goes high. On the following rising edge of T_f, the second register keeps the value of Q_1 and switches Q_2 to high. When the signal edge of T_1 catches up with T_2, the output QD_1 rises and switches the output of the AND gate to generate the Phase Detected signal, as shown in Figure.3. The Phase Detected signal is fed to the counter where it stops the time measurement process.

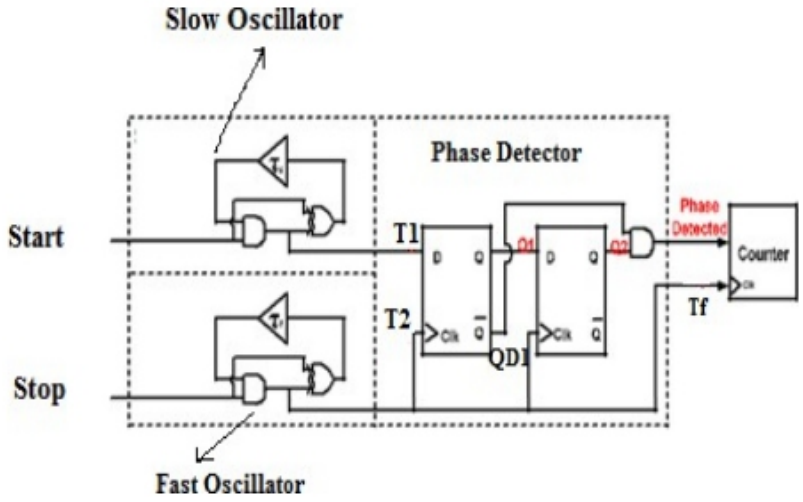

Fig.3. Block diagram of proposed TDC

Resolution is the difference of slow clock and fast clock, and the meta-stability is likely to happen in the phase detector, when the T_1 signal catches up with T_2Signal and the phase difference between these two signals is smaller than the required setup time.

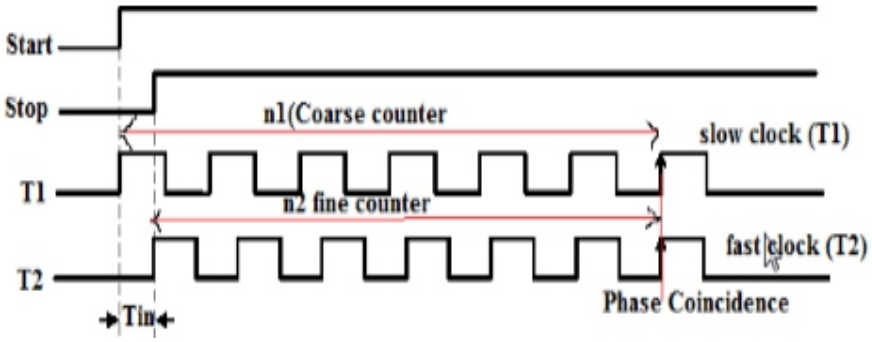

Fig.4. Timing diagram of the phase coincidence

The resolution is the time difference between slow oscillator time period and fast oscillator time period, and it is defined

By-

Resolution® = $T_s - T_f$

$$T_{in} = (n_1\text{-}1)\, T_1 \; - (n_2\text{-}1)\, T_2 \qquad (1)$$

$$= (n_1\text{-}n_2)\, T_1 + (n_2\text{-}1)\, R \qquad (2)$$

When $T_{in} < T_{slow}$, then $n_1 = n_2$ and T_m is given by

$T_{in} = (n_2\text{-}1)\, R$

Where,

T_1 = Time period of slow oscillator

T_2 = Time period of fast oscillator

n_1 = counted number of slow clock

n_2 = counted number of fast clock

Resolution of the system = $T_1 - T_2$

IV. SIMULATIONS AND RESULTS

The simulations are performed using ISE Xilinx software.

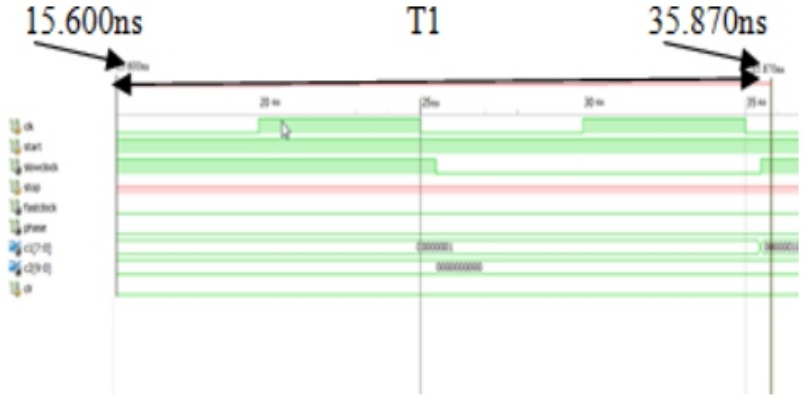

Fig.7. Output waveform of slow oscillator

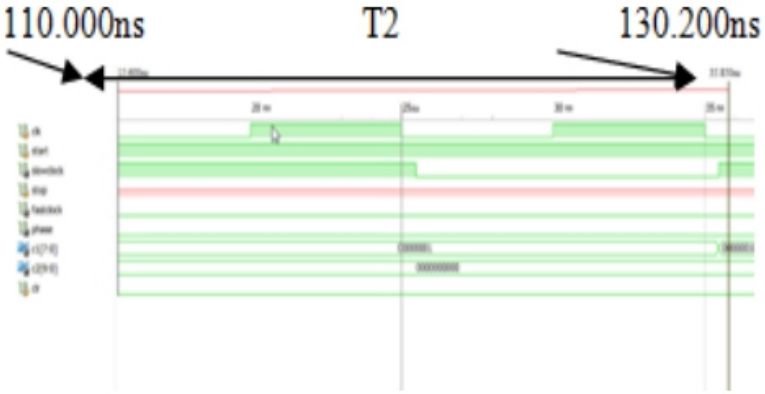

Fig.8. Output waveform of Fast oscillator

The result of start & stop clock is given above fig.7& Fig.8.

Specification	Value
Slow oscillator period (T1)	20.270ns
Fast oscillator period (T2)	20.200ns
Resolution $\Delta\tau = T_1 - T_2$	70ps

Table I: TABULATED VALUES OF THE TEST RESULTS

Design Parameters	Earlier work by [11]	Earlier work by [2]	Earlier work by[8]	Proposed Design
Time Resolution (ps)	1ns	200ps	160ps	70ps
Structure	Vernier	Vernier	Vernier Ring Oscillator	Vernier Ring Oscillator
Device	FPGA	FPGA	FPGA	FPGA

Table II: COMPARISON OF RESULTS OF PROPOSED DESIGN WITH EARLIER DESIGN

V. CONCLUSIONS

It is hard to get TDC with few picoseconds resolution in FPGA paradigm. The purpose of this work was to develop a time-to-digital converter architecture with a fine and coarse counter achieved high resolution, low power consumption, small area and low cost. This paper reports optimization of area as well as reduce the floor planning burden. Hence it is an area efficient TDC useful for the application mentioned in[10]. Our Vernier techniques resort to maintain stable resolution of 70ps. Vernier delay ring architecture is folded back to its beginning to increase the dynamic range without adding more delay elements and also achieves low power consumption.

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Traffic Prediction System in AOMDV Protocol using Vanet Environment

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ABSTRACT

The Vehicular Ad-Hoc Network, or VANET, is a expertise that customs moves cars as nodes in a network to create a mobile network. VANET turns every linking car into a wireless router or node, allowing cars nearly 100 to 300 meters of each other to connect and, in turn, create a grid with a wide range. As cars drop out of the signal range and dewdrop out of the network, other cars can join in, involving vehicles to one another so that a mobile Internet is created. Ad- hoc On-demand Multipath Distance Vector (AOMDV) protocol is used for investigating the traffic expectation in VANET environment based of different parameters. The parameters like packet delivery ratio (PDR), End to End delay, Throughput, Different Running Time and so on. VANET environment is created by using SUMO tools and performance analyses using NS2.35

Keywords - VANET, AOMDV, PDR, End to End Delay, Throughput and SUMO

I. INTRODUCTION

The main idea in AOMDV is to compute several paths for the duration of route discovery. It is designed primarily for highly dynamic ad hoc networks where link failures and route breaks occur frequently. When particular path on-demand routing protocol such as AODV is used in such networks, a new route discovery is required in rejoinder to every route break. Each route discovery is associated with high-overhead and latency. This inefficiency can be avoided by having multiple redundant paths available. Now, a new route discovery is needed only when all paths to the target break. A noteworthy feature of the AOMDV protocol is the use of routing information already available in the underlying AODV protocol as much as possible. Thus little additional overhead is required for the reckoning of multiple paths. The AOMDV protocol has two main constituents: 1. A route update rule to establish and maintain multiple loop-free paths at each node. 2. A distributed protocol to find link-disjoint paths.

II. AOMDV

It work to compute multiple paths during route discovery procedure for contending link failure. When AOMDV builds multiple paths, it will select the main path for data transmission which is based on the time of routing establishment. The earliest one will be regarded the best one, and only when the main path is down other paths can be effective. In fact, a large number of studies indicate that the aforementioned scheme is not necessarily the best path. Mobile nodes, which usually due to residual

energy are too low or under heavy load and other factors, seriously affect the performance of the network. First it considers the rate of node residual energy and idle buffer queue as the weight of node.

Second, in route discovery process, the routing inform rules estimate the node weight of each path and sort the path burden by descending value of path weight in route list, and they choose the path which has the major path weight to transmit data packets. At the same time, the protocol uses the machinery of RREQ delay forwarding[1, 2] and energy edge to ease network congestion, limit the RREQ announcement storm, and avoid low energy nodes to join in the establishment of the path [1].

III. RELATED WORK

Mahesh K. Marina et.al[3] says multipath routing can be used in on-demand protocols to achieve faster and efficient recovery from route failure in highly dynamic ad hoc networks. They have proposed an on- demand, multipath distance vector protocol AOMDV that expands the single path AODV protocol to compute multiple paths. There are two main contributes of this work they use the notion of an advertised hop count to maintain multiple loop-free paths each node. It show how route discovery mechanism in the AODV protocol can be modified to obtain link disjoint multiple paths from source and alternate notes to destination.

Jieying Zhou et.al[1] Implies a novel multipath distance vector routing protocol, NS-AOMDV, for MANETs is projected to improve some shows of present AOMDV. In the process of building program path, synthetically consider the residual energy rate and the idle rate of buffer queue. And announce the technology of RREQ delay hold back and energy threshold in route discovery. Also update the information of the nodes on the path, and choose the path of maximum node weight for data transmission. It introduce the concept of Node State AOMDV (NS- AOMDV) and analysis various parameters like Pausetime, End to End Delay, Routing Overhead, Moving Speed of the node and so on. Preeti Aggarwal [4] Et.al has studied the various aspects of AOMDV protocol. After studying the various aspects of AOMDV they have concluded that AOMDV has many advantages but there are some shortcomings in AOMDV which needs to be improved to improve the performance of Manet.

Geetha S, Dr. Geetharamani et al.[5] had taken random way point mobility model in order to question the performance enhancement of AOMDV with energy efficient routing. Each node in MANET will maintain the information required for proper route traffic. In order to improve the performance of AOMDV in selecting main path, new concept is proposed in this paper called Node state with mobility model (NS-AOMDV). The simulation results showed that the proposed method (NS-AOMDV) had significant reliability improvement as compared to AOMDV.

Simulation work Simulation Parameter:

Parameters	Value
Simulator	**Ns.2.34**
Simulation time	**1000 ms**
Number of nodes	**10**
Routing protocol	**AOMDV**
Simulation Area	**1000*1000 m**
MAC Protocol	**IEEE802.11**
Channel Type	**Wireless**
Antenna Type	**Omni Antenna**

IV. RESULT AND ANALYSIS

A. Packet Delivery Ratio:

The packet delivery ratio is defined as total number of received data packets divided by the number of generated data packets.

$$\textbf{PDR} = \Sigma \text{ Number of Packet Receive} / \Sigma \text{ Number of Packet Send}$$

$$= 98.8665\ \%$$

B. End to end delay:

The end to end delay defined as the time a data packet is received by the destination minus the time the data packet is generated by the source.

$$EED = \frac{1}{k} \sum_{i=1}^{K} \frac{tdD}{ndpD}$$

$$= 138.68 \text{ ms}$$

Where,

- tdD -Total delay of packets received by the destination node
- ndpD- The number of packets received by the destination node
- k- Network traffic.

C. Throughput:

The throughput is defined as average ratio of the successful packets delivered to particular destination to those of generated by the traffic sources. This is measured as bits per second.

$$TP = \left(\frac{ReceiveSize}{Stop\ Time - Start\ Tim}\right) \times 8/1000$$

$$= 284.52NS$$

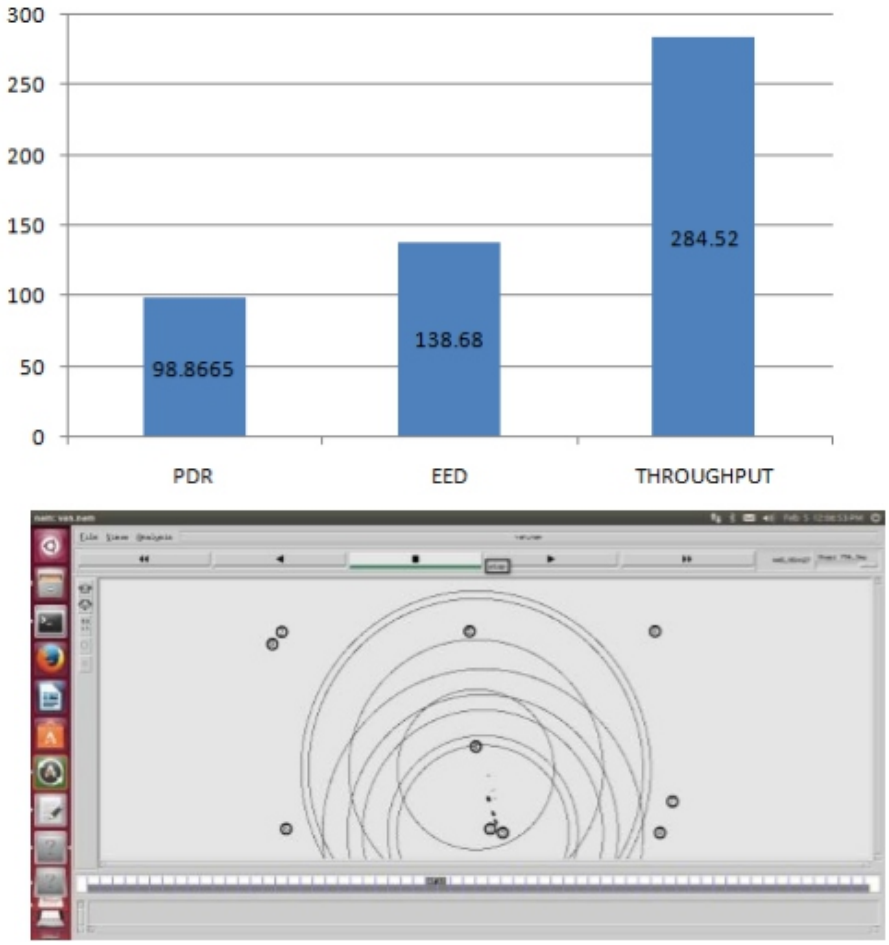

Fig 7: Graphical view for NS2 tool Simulation for Network Traffic

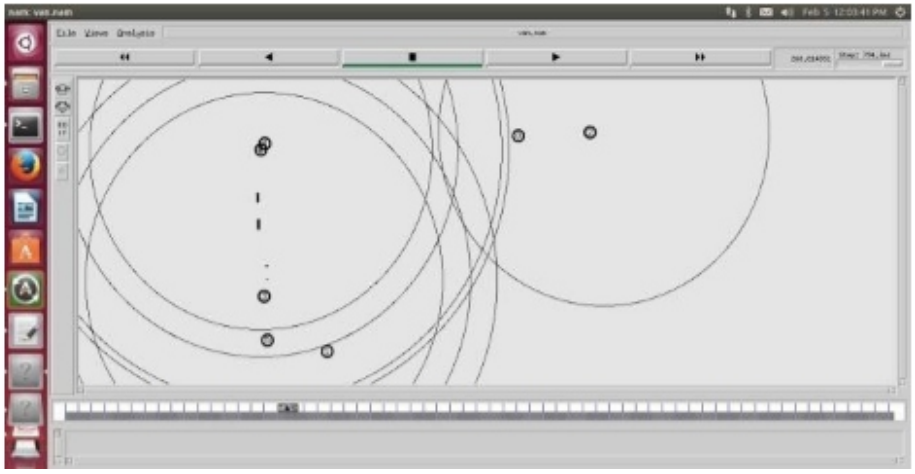

Fig 8: Finding Alternate Path using AOMDV Routing Protocol

V. CONCLUSION

In AOMDV protocol is used for finding another pathEED = when existing path was broken or any other issue to next high priority node at presented in updated table. This table keeps a data about nearest node, node position and other related information in dynamically. Then it analysis this protocol using various parameter like Throughput, End-to-End Delay and delivery ratio it gives good performance. In future it

will discuss about various different protocols with multiple parameters like Jitter, QoS and also implement different type of mobility model.

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Comparative Study of SPI Design Systems

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ABSTRACT

There's a specialized chip-selection signal used for addressing and controlling an individual slave in most frequent SPI schemes with one master and several slaves arrangement that we can meet when design. But the complication of such a scheme is that if the number of slaves increases in the circuit, there are also more chip-select lines and the circuit becomes complex and this is difficult to design. In such a situation, maintaining the minimality of the design becomes a challenge. A developer can use other techniques, such as daisy chaining with fewer terminals on the master computer but with the significant lack of a small bandwidth for communication. A comprehensive comparison research with general SPI and Daisy-chained SPI systems is described in this paper.

Keywords - Intellectual Property Core, Serial Communication, Serial Peripheral Interface, SOC

I. INTRODUCTION

As stated, in SPI circuit there is one master and there can be multiple slaves. This master slaves configuration can be implemented by two methods:

1. Regular SPI Multislave Configuration.
2. Daisy wheel configuration

A. Regular SPI Multislave Configuration

There is a single master in this mode and multiple chips for the individual slaves are necessary from the master. The data and clock on the MISO / MOSI lines are available on the MISO / MOSI lines when the chip select signal is activated by this slave master for a particular slave. The drawback this paper intends to identify is noted when multiple chip select signals are activated simultaneously for each slave in the same time. The MISO information is broken because the master doesn't recognize which slave sends the data. As seen in the adjacent figure1, with each slave the number of selected lines increases which means the complexity of the circuit increases as the number of slaves increases. This increase in the number of slaves that can be connected on the circuit in the output lines required by the master for every slave. A MUX for generating a chip select signal is one way to boost the amount of slaves to be used in normal mode.

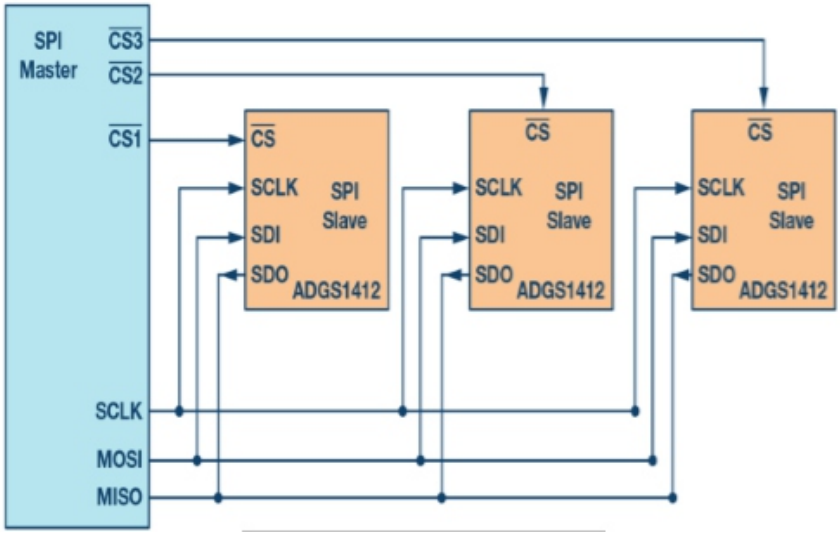

Fig 1. SPI regular method

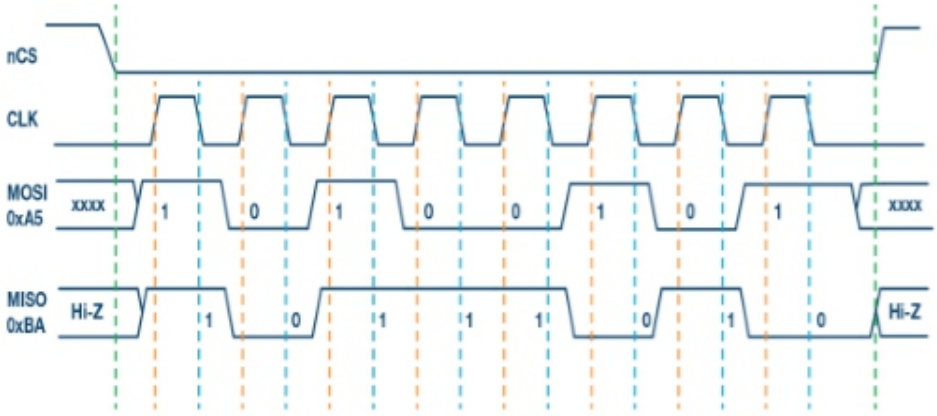

Fig:2 Regular SPI Timimg Diagram

Illustration 2. SPI mode, sampled on increasing rim and shifting to falling edge, CPHA= 0: CLK idle state= low.

Illustration 2. Overview demonstrates the prevalent SPI mode procedure by sampling the information on the upward edge and shifting on the downward edge. Data on the MOSI and MISO lines are shown in this figure. The transmission beginning and end are shown by the pointed green line, the bottom of the sample is marked orange and the bottom is specified in blue.

B. Daisy Chain Method

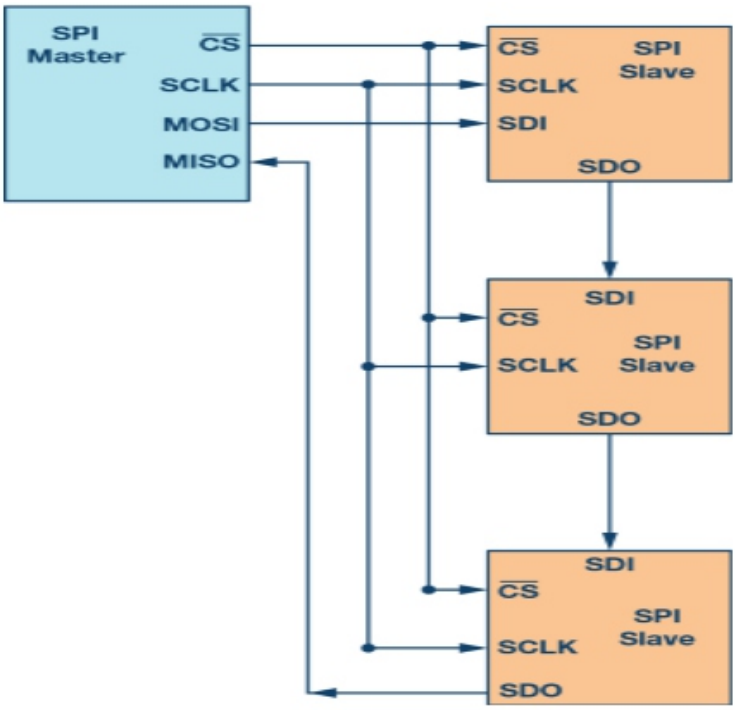

Fig3 SPI Daisy chain Block Diagram

The slaves are configured in the daisy chain mode to link the chip select signals for all the slaves and to propagate data from one slave to the next. Every slave gets the same SPI clock in this setup simultaneously. The master data are linked straight to the first boy and that boy gives the next boy and so on. In this configuration all data sent by the master is shifted into all devices and all data sent from each device is shifted out to the next. Figure 4 shows the clock cycles and data propagating through the daisy chain.

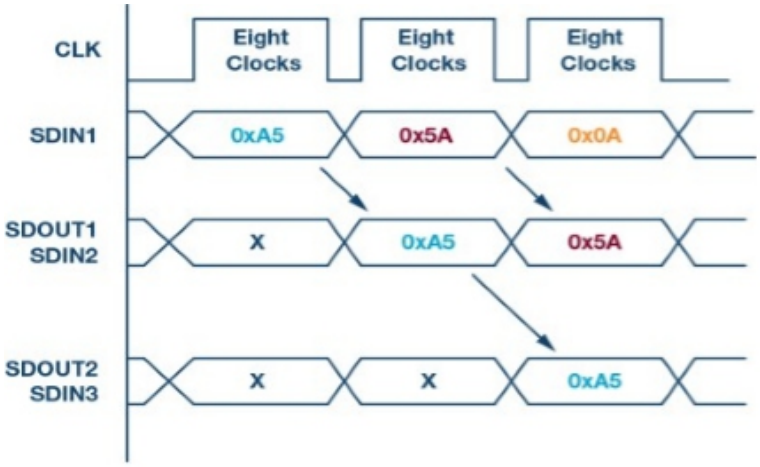

Fig4. Daisy-chain configuration: data propagation.

Simulation Result:

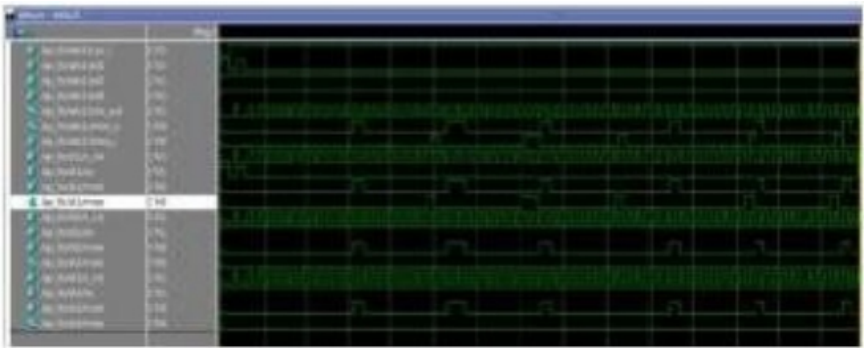

Fig5. Regular SPI Timing Diagram

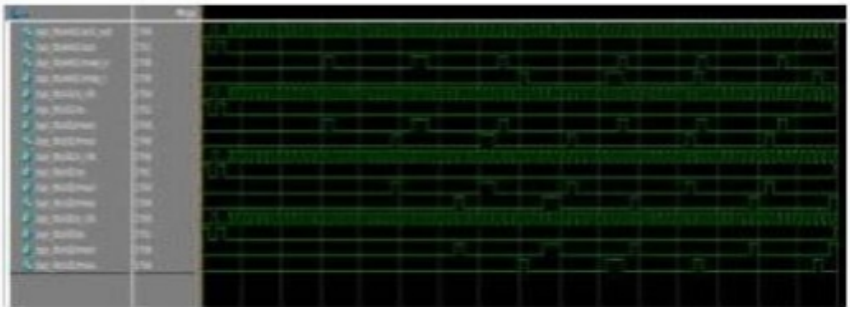

Fig6 SPI Daisy chain Timing Diagram

II.CONCLUSION

The comparative study carried out shows that the circuit becomes much more complex and difficult to implement because of the higher number of chip selector lines required in the regular SPI configuration and thus has smaller applications while the daisy wheel configuration is much less complex and easier to implement, if the number of the slaves required is much less than the number of chip select lines required.

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Gas Leakage Detection and Accident Prevention System using IOT

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ABSTRACT

IoT is an extending system of physical gadgets that are connected with various sorts of sensors and with the help of availability to the web, they can trade information. Through IoT, web has now stretched out its underlying foundations to pretty much every conceivable thing present around us and is not any more constrained to our PCs and cell phones.

Security, the rudimentary worry of any undertaking, has not been left immaculate by IoT. Gas Leakages in open or shut regions can turn out to be perilous and deadly. The conventional Gas Leakage Detector Systems in spite of the fact that have incredible accuracy, neglect to recognize a scarcely any elements in the field of alarming the general population about the spillage. In this manner we have utilized the IoT innovation to make a Gas Leakage Detector having Savvy Alerting systems including calling, sending instant message and an email to the concerned expert and a capacity to foresee unsafe circumstance with the goal that individuals could be made mindful in advance by performing information examination on sensor.

Keywords - Internet of Things, Gas Leakage Detector, Raspberry Pi, Data Analytics.

I. INTRODUCTION

The Internet of Things is a developing subject of specialized, social, and monetary importance. Shopper items, solid merchandise, vehicles and trucks, modern and utility parts, sensors, and other regular articles are being joined with Internet network and ground-breaking information scientific abilities that guarantee to change the manner in which we work, live, and play. Projections for the effect of IoT on the Internet and economy are amazing, with some foreseeing upwards of 100 billion associated IoT gadgets and a worldwide monetary effect of more than $11 trillion by 2025. The Internet of Things (IoT) is an essential theme in innovation industry, approach, and building circles and has moved toward becoming feature news in both the claim to fame press and the well known media. This innovation is encapsulated in a wide range of organized items, frameworks, and sensors, which exploit headways in figuring power, gadgets scaling down, and arrange interconnections to offer new abilities not beforehand possible IoT frameworks like organized vehicles, clever traffic frameworks, and sensors installed in streets and scaffolds draw us nearer to "keen urban communities", which help limit clog and vitality utilization. IoT innovation offers the likelihood to change farming, industry, and vitality generation and dissemination by expanding the accessibility of information along the esteem chain of creation utilizing organized sensors.

II. RELATED WORK

Gas Detectors have been in the market for a very long time and have been immeasurably utilized. They have wide scope of uses and can be found in mechanical plants, refineries, pharmaceutical assembling, paper mash factories, airplane and ship-building offices, wastewater treatment offices, vehicles, indoor air quality testing and homes[2]. There are a great deal of manners by which the Gas Detectors could be described. They are ordered on the premise of what sort of gas they identify, what is the innovation behind the creation of the sensor and some of the time even the parts which are utilized that influence their activity component (semiconductors, oxidation, reactant, photoionization, infrared, etc.)[2]. Gas Detectors are additionally broadly portrayed as fixed or versatile indicators. They are portrayed based on which class of hazard they fall in, Ex- Bull Tox, the three classifications of hazard - Ex – Risk of blast by combustible gases - Ox – Oxygen Risk of suffocation by oxygen relocation Risk of increment of combustibility by oxygen advancement – Tox – Risk of harming by dangerous gases [3], the rundown of classification goes on. Subsequently we can't have a single framework or a gathering of frameworks which we can call the best however rather there is a plenty of gadgets accessible for coordinating the differing client necessities some of which are recorded underneath.

A. Handheld EGD01

This Handheld EGD01 conveys high-affectability, and is effectively customizable for distinguishing a wide assortment of flammable gases, including methane, propane, and butane. It is utilized by the building auditors [4]. As the name of the item recommends, it is a versatile gadget and henceforth battery worked. It has both a sound and light caution.

B. Amprobe GSD600 Gas Leak Detector

This is a versatile gas identifier for distinguishing gases for example, methane and butane. It has a tempered steel test. The test enables the client to get into the hard to- achieve places. It was intended for recognizing gas inside shut funneling framework and it has a discernable alert [4].

C. Analox Sensor Technology

Security of grounds as far as gas spillage identification in research center condition, flasks and different zones of conceivable gas spillage have been guaranteed by utilizing of gadgets, for example, O2NE+, SAFE-OX+, A50, and so on.

Given by ANALOX Sensor Technology [5] and a lot increasingly such gadgets by different makers are utilized all around the globe in all the grounds.

Our IoT based model for gas spillage identification is taking this conventional approach a score up by including the component of promptly insinuating the concerned experts and additionally refreshing the sensor readings, time to time, on cloud. The itemized depiction is given in Section 4 of this paper.

III. SMART HOMES AND CITIES

Web of Things is being utilized wherever all together to facilitate our day by day assignments and improve the personal satisfaction.

There are multitudinous modules that could be thought of for savvy homes and urban communities and some of them are talked about beneath:

A. Gas Detection Systems

This is the framework which has been talked about in this paper. The adaptable idea of this framework comes due to the way that a similar framework with an adjustment in the type and number of sensors can be utilized in various places. They can be utilized at homes, structures, enterprises for identifying LPG, Propane, Methane or some other unsafe gas spillages (talked about in this paper) and with certain progressions could be utilized in urban communities for distinguishing air contamination and performing investigation on the sensor readings to anticipate and forestall risky circumstances.

B. Traffic the executives framework

In London, a traffic the executives framework known as Hurry boosts green light time at traffic crossing points by nourishing back magnetometer and inductive circle information to a supercomputer, which can coordinate traffic lights over the city to improve traffic throughput.[6]

C. Brilliant Lighting

Adaptable road lighting (brilliant lighting) [7] permits regions to control the splendor of road lights.

D. Voice Controlled Automation

The business items Google Home and Amazon Reverberation are as a rule generally utilized for computerization of home.

These improve nature of living just as consider the vitality preservation factors, for example, turning off lights and fans consequently when the room is void.

IV. GAS LEAKAGE DETECTORS

Distinctive sorts of supplies are utilized for different purposes in our everyday life and the greater part of them have the ability of discharging some sort of gases or a few mixes noticeable all around while being used. It is very critical to keep a beware of the fixation levels of the gases and different mixes as some of them, at the point when surpass the protected fixation level, are combustible under the room temperature and dampness condition. Blends of scattered ignitable materials, (for example, vaporous or vaporized energizes, and a few tidies) and air will consume just if the fuel fixation exists in all around characterized lower and upper limits decided tentatively, alluded to as combustibility limits or hazardous breaking points. Ignition can extend in savagery deflagration, through explosion, to blast [10].

A customary gas location framework checks for the fixation levels and cautions individuals about the spillage through sound and visual alerts. The IoT based model of the customary gas spillage discovery framework does not just cautions individuals by sound caution yet in addition endeavors to alarm the concerned work force through a call and instant message on their telephone so that regardless of whether nobody is available in the territory of spillage, they are made mindful of the circumstance. Alongside this the model additionally sends the subtleties sensor perusing recorded when the caution got incited which could be utilized by an individual or an association to settle on choice about what sort of consideration is required in the territory of gas spillage.

Another most huge element of this model is that it can record the sensor readings and keep up a database of these readings of centralizations of gases at various timestamps. This information could be used for completing investigation on it. The examination of the sensor readings can help in comprehension the standard thing states of the territory, under what conditions do the readings of sensor more often than not goes up and when does it as a matter of fact begin getting risky and needs consideration. This will build the accuracy of the framework, lessening the bogus cautions and consequently really turning into an entirely dependable framework inside a range of a barely any days. Alongside every one of these highlights, this framework additionally accompanies a power cut off alternative. In the event that the grouping of combustible gases is going to reach their lower unstable farthest point (LEL) the framework trips the fundamental switch which causes a total power cut off of the building or office or wherever theframework is introduced. This will fill two need that is one, it will keep any fiasco because of power or power what's more, two, in the event that the spillage is being brought about by any gadget whose killing will keep any further spillage, this reason will be served by the control cut off component. Portrayal about the segments utilized and the handling steps included have been talked about in detail in Section 4.1 and Segment 4.2 of this paper.

Components:

The fundamental segments utilized really taking shape of this model are as per the following:

1) Raspberry Pi Module: Raspberry Pi resembles one of the Microcomputers. The Raspberry Pi 2 speaks to one of the best of its sorts. Most importantly, it utilizes Linux Operating Framework. This Microcomputer is utilized in each field now adays;[9] they are incredible for instruction extends and even to run numerous cutting edge games.[11]It is upheld on Raspbian Working System (OS) and it utilizes Python as primary programming Language. Raspberry Pi Module 2 is shown.

2) GPS Module: Global Positioning System (GPS) makes utilization of signs sent by satellites in space and ground stations on Earth to precisely decide their situation on Earth. Radio Frequency signals sent from satellites and ground stations are gotten by the GPS. GPS makes utilization of these signs to decide its definite position. The GPS itself does not have to transmit any data. The signs got from the satellites and ground stations contain time stamps of when the signs were transmitted. By ascertaining the contrast between when the flag was transmitted and when the flag was gotten. Utilizing the speed of the flag, the separation between the satellites and the GPS collector can be resolved utilizing a basic recipe for separation utilizing rate and time. Utilizing data from at least 3 satellites, the precise position of the GPS can be triangulated.

3) GSM Module (SIM900A): This module is associated with Raspberry Pi board which helps in making calls and sending instant messages when the sensor esteem crosses as far as possible.

The SIM900A conveys GSM/GPRS 900/1800MHz execution for voice, SMS, Data, and Fax in a little structure factor and with low power utilization [13].

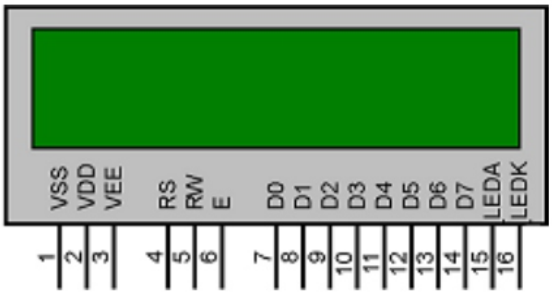
4) Gas Sensor-MQ6: In this, we will utilize MQ6 Gas Sensor. It has high affectability to LPG,iso-butane and propane. It counters in all respects rapidly and proficiently. It even has a long life. MQ6 Gas Sensor is appeared in fig 3.

Favorable circumstances of MQ6 Sensor:

- They can be utilized to distinguish gas spillage in Industries and Houses.
- It has a basic drive circuit.
- A green drove is activated after the recognition of gas.

Fig 3 .MQ6 Gas Sensor

5) LCD Display: 16x2 LCD display is used to display the gas concentration values.



6) Relay: Relay that works with 220V and has a 5V input is utilized in the circuit for cutting off power when required. The hand-off has 5 pins. One stick is associated to one of the advanced pins of the Raspberry Pi Board. One is associated with scaffold the 220V power supply to the hand-off. The other stick diverts this supply to the machines. Rest of the two are ground association, one for the primary power supply and the other for Raspberry Pi Board.

7) Piezo Buzzer: It is utilized for creating sound caution.

Software Requirement:

Python Programming: Python is an amazing programming language that is even extremely simple to use with Raspberry Pi. It even uses less lines of codes as contrasted with C or C++. In our task, we use Python in request to make associations with Raspberry Pi 3.

System Implementation:

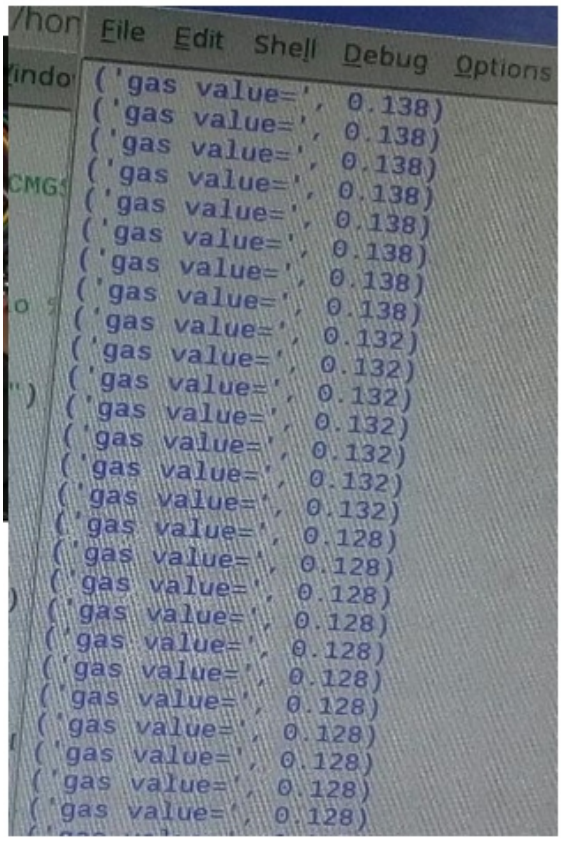
Working:

1) The sensors are interfaced with Raspberry Pi module, the input to the kit are MQ-6 sensor. The output is given to LCD display and Buzzer.
2) GSM module is also connected with Raspberry Pi to connect with user.
3) After turning ON the application, MQ-6 gas sensor starts detecting gases present in environment and their concentration.
4) As it detects hazardous gases like LPG, propane, etc., it gives alert to the respective authority using GSM module.
5) At every instant, the gas name and it's concentration is displayed on the LCD display.
6) As per requirement of industry, we will set a set point for the concentration of different gases.
7) If the gas concentration reaches near to set point, buzzer will turn ON and the alert message will send to the respective authority and the plant will stop there itself.
8) After stopping the plant, water sprinklers and the exhaust fans will turn ON.
9) Then message will send to the fire brigade. It will come to know the location of the plant using GPS model.

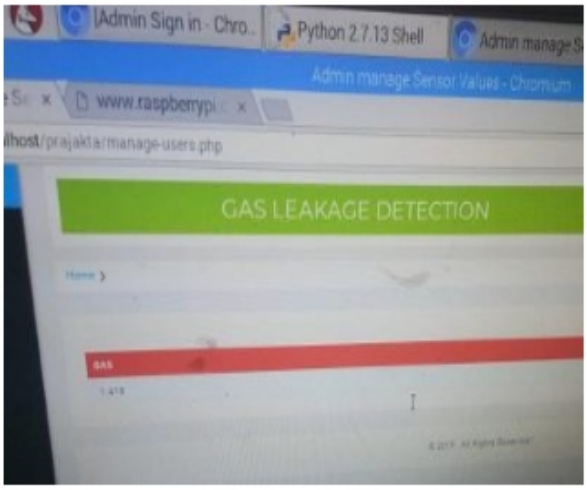
V. RESULT

As we start the system, it will sense the gases in environment and display their concentration on LCD display. We have set the threshold value as 1 ppm. When the gas concentration reaches to threshold value the buzzer will turn ON and alert message will sent to respective user.

In output, we get different values of gas concentration as shown below.



We have created the webpage which shows the concentration of gas at every moment. The user can get the status of gas concentration through this webpage.



VI. CONCLUSION

This system is designed for industries and family unit condition for gas leaks and increment in temperature. The framework ceaselessly screens the qualities also, acts in like manner to limit chance. Being cost successful, it very well may be actualized in different conditions. The alert is sent to authority when values exceed the threshold value. The gas and temperature esteems alongside time and date can be seen on a webpage.

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