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Journal of Electrical Engineering and Advanced Technology

Aims and Scope

Journal of Electrical Engineering and Advanced Technology is a journal that publishes original research papers in the fields of Electrical Engineering and Advanced Technology and in related disciplines. Areas included (but not limited to) are electronics and communications engineering, electric energy, automation, control and instrumentation, computer and information technology, and the electrical engineering aspects of building services and aerospace engineering, Journal publishes research articles and reviews within the whole field of electrical and electronic engineering, new teaching methods, curriculum design, assessment, validation and the impact of new technologies and it will continue to provide information on the latest trends and developments in this ever-expanding subject.

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Contents

Theoritical Aspects of Asynchronous Circuit Design to Reduce Power Consumption in A VLSI

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A B S T R A C T

This paper starts by depicting the real favorable circumstances of utilizing asynchronous VLSI designs and gives an outline of the asynchronous design methodologies and techniques grew up until this point. Ensuing segments show portrayals of the micro pipeline and handshake circuit design methodologies which are the fundamental asynchronous design styles utilized as a part of the work depicted in this paper. The importance of creating asynchronous design for testability (DFT) techniques is examined. At last, the last segment contains a paper review depicting the structure of this and the results distributed by the creator.

1. ASYNCHRONOUS VLSI CIRCUITS

Asynchronous circuits communicate via handshakes. A handshake consists of a series of signal events sent back and forth between the communicating elements. We can divide the communicating elements into a sender and a receiver part. The sender is the element that initiates the handshake sequence. If the sender wants the receiver to perform a certain task, it makes a request to the receiver. When the receiver has finished executing the task it make an acknowledgement to the sender that the task has been completed. This is the way sequencing of actions is handled in asynchronous circuits - by handshake communications.

Very Large Scale Integration (VLSI) circuits designed utilizing modern Computer-Aided Design (CAD) tools are ending up quicker and larger, consolidating a huge number of littler transistors on a chip. VLSI designs can be partitioned into two noteworthy classes: synchronous and asynchronous circuits. Synchronous circuits utilize global clock signals which are conveyed throughout their sub circuits to guarantee remedy timing and to synchronize their data processing mechanisms. Asynchronous circuits contain no global clocks. Their operation is controlled by privately produced signals [1].

2. MOTIVATION FOR USING ASYNCHRONOUS CIRCUITS

A resurgence of enthusiasm for the design of asynchronous circuits has been fortified by their potential favorable circumstances contrasted with their synchronous partners[2]:

- **The non-appearance of the clock skews issue.** The largest issue with clocking in VLSI circuits lies in dispersing the clock at a similar moment to all clocked elements over the chip. "Clock skew" depicts the marvel whereby diverse parts of the VLSI framework see the clock at marginally extraordinary circumstances because of defer varieties in the clock interconnections. Clock dispersion plans which limit the clock-skew window turn out to be increasingly exorbitant in modern VLSI designs [3]. This is on the grounds that modern condition of workmanship VLSI technology tends to utilize littler transistors in larger chips which expand the importance of physical postponements along wires in a chip instead of signal deferrals through transistors.

- **Performance.** The settled clock time frame in synchronous circuits is picked utilizing most pessimistic scenario performance analysis. As an outcome, synchronous circuits perform even from pessimistic standpoint case rates. In asynchronous circuits, the communication between independent blocks on the chip happens when the data is prepared to be transmitted. As a result, asynchronous designs can exhibit regular case performance instead of most pessimistic scenario performance.

- **Power consumption.** The power consumption of VLSI circuits is important in portable computerized frameworks since a design objective is to boost the life of lightweight battery packs. All parts of a synchronous VLSI design are clocked regardless of whether they don't create "valuable" results. In asynchronous circuits, just those parts of the circuit which deliver important results are associated with the calculation procedure. As a result, the utilization of asynchronous circuits can prompt lower control consumption.

- **Timing and design adaptability.** In the event that a synchronous VLSI circuit is required to work at a higher clock recurrence, all parts of the circuit must be enhanced to work inside the shorter clock time frame. In an asynchronous circuit, performance can be upgraded by changing just the most dynamic parts of the design utilizing advancements in VLSI technology. Since asynchronous circuits convey utilizing signaling protocols instead of clocks the changed parts should just comply with the prerequisites of the communication protocol [4].

3. ASYNCHRONOUS VLSI DESIGN METHODOLOGIES

Countless asynchronous design methodologies can be characterized utilizing the accompanying three primary criteria:

- Delay models;
- Data representation;
- Signaling protocols.

DELAY MODELS IN VLSI CIRCUITS

Delay models can be partitioned into three classifications: settled, bounded and unbounded delay models. In the settled delay model, the delay is assumed to have a settled esteem. As indicated by the bounded delay model the delay may have any an incentive in a given interim. In the unbounded delay model, the delay can have any limited esteem. Delays in computerized circuits are related with wires and gates. On a basic level, a circuit model is characterized by its function and delay models for its wires and parts [5].

- In delay-insensitive circuits all delays in gates and wires are permitted to be arbitrary yet limited.
- Gate delays in speed-autonomous circuits are arbitrary and limited yet signal transmissions along wires are quick.
- A bounded-delay circuit utilizes the bounded delay model to guarantee amend data processing. In this model the delays through the data paths of the circuit are known and bounded while the control logic remains delay-insensitive.

DATA REPRESENTATION

Data in asynchronous circuits can be spoken to utilizing either dual-rail or single-rail data encoding.

Both delay-insensitive and speed-autonomous implementations require dual-rail encoding of data where every datum bit is spoken to by two wires: a "zero" engendering wire and a "one" spread wire. A standard level-delicate dual-rail data encoding system has four states.

- 00 - “initial state; data is not valid”;
- 10 - “transmission of a logical zero”;
- 01- “transmission of a logical one”;
- 11 - “Illegal state”.

SIGNALING PROTOCOLS

Most asynchronous communications depend on utilizing signaling protocols which characterize a "handshake" method between two calculation blocks [6].

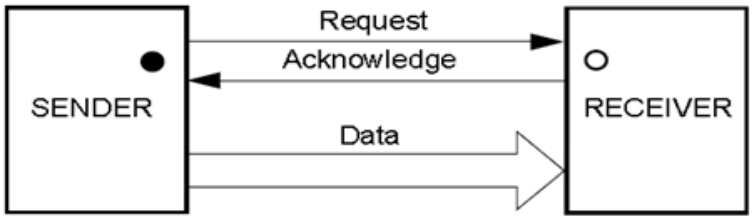

Figure 1: Standard handshake signaling protocol

The full and purge hovers in Figure 1indicate the dynamic and the passive accomplices in the handshake methodology separately. Two transition signaling plans can be utilized to actualize an asynchronous signaling protocol: two-stage (non-come back to zero) and four-stage (come back to zero) signaling. Figure 2 represents the two-stage packaged data signaling protocol.

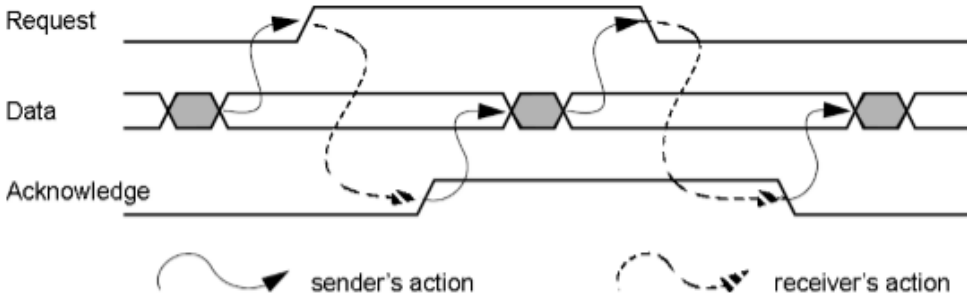

Figure 2: Bundled-data protocol using two-phase transition signaling in Figure 1

There are two dynamic stages in the communication procedure: the signal transitions (rising or falling) on the request and acknowledge wires.

Amid the receiver's dynamic stage the sender must hold its data unaltered. Once the receiver creates an acknowledge occasion new data can be delivered by the sender. In Figure 2 strong and dashed lines speak to the sender's and the receiver's activities individually.

4. ASYNCHRONOUS DESIGN STYLES DELAY-INSENSITIVE CIRCUITS

The acquainted techniques with execute delay-insensitive circuits which can be either without clock or privately clocked (Q-modules). Abnormal state depiction dialects, for example, Occam and a follow based dialect were utilized by Brunvand and Ebergen separately to design module- based delay-insensitive circuits.

Extraordinarily created programmed aggregation strategies are connected to the abnormal state design depiction keeping in mind the end goal to actualize a delay-insensitive circuit [7].

QUASI DELAY-INSENSITIVE AND SPEED-INDEPENDENT CIRCUITS

Martin proposed a methodology for designing alleged semi delay-insensitive circuits which vary from speed-autonomous circuits for the most part in the assumption that all forks in speed-free circuits are isochronic, though semi delay-insensitive circuits enable forks to be either isochronic or delay-insensitive. The design procedure incorporates two fundamental advances. The creating of the abnormal state determination utilizing the imparting successive procedures (CSP) dialect;

- The interpretation of the abnormal state particular into a circuit implementation. Philips explores research facilities built up the Tangram programming dialect which is like CSP. An arrangement of tools accommodating the assemblage of the Tangram program in a handshake circuit has been executed.

A few reports proposed various design techniques for speed-autonomous circuits. These design approaches depend on the abnormal state circuit determination as signal transition diagram (STG)[8].

BOUNDED-DELAY CIRCUITS

Bounded-delay circuits utilize the central mode assumption that the environment must sit tight for a considerable length of time for the output data to balance out on the circuit outputs. The standards of major mode design techniques were produced first by Huffman and later stretched out by Unger [9].

As per this approach:

- Each state transition can happen under a specific arrangement of input changes (purported an input burst) so no burst from a specific state can be a subset of another burst from a similar state;
- Any state must be entered with a similar arrangement of input values. The proposed timing mechanism permits the burst-mode limited state machine to be moved to another state at whatever point the output related with the past state has changed empowering the input signals to be changed.

Ivan Sutherland in his 1988 Turing Award address depicted a rich way to deal with building asynchronous pipelines called micro pipelines. Micro pipelines are asynchronous, occasion driven pipelines in view of the packaged data interface. In micropipelines, the data is dealt with as a package, i.e. at the point when the data created by the sender is steady the sender issues a request occasion to the receiver; the receiver acknowledges the receipt of the data by sending an acknowledge occasion. This handshaking mechanism is rehashed when facilitate data is delivered by the sender [10].

5. CONCLUSION

Current results acquired so far in the field of testing asynchronous circuits are examined. This incorporates an analysis of reports committed to fault modeling in asynchronous VLSI circuits, test generation techniques and design for testability strategies for delay-insensitive, speed-free and bounded-delay circuits. Two generations of asynchronous RISC processor (AMULET1 and AMULET2) have been designed by the AMULET look into gathering. Issues identified with the testing of asynchronous circuits have been to a great extent overlooked. As a result, the business value of the AMULET designs, which requires viable test systems to be connected to chips produced in high volume, stays low.

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Grid Integration Inverter and Power Quality Issues of Windturbine Technology, Solar Energy System

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ABSTRACT

This paper emphasize on grid integration inverter and power quality issues of wind turbine technology, solar energy system. The expanding number of renewable energy sources and dispersed generators requires new strategies for the operation and administration of the electricity grid with a specific end goal to keep up or even to enhance the power-supply unwavering quality and quality. What's more, progression of the grids prompts new administration structures, in which exchanging of energy and power is winding up progressively imperative. The power-electronic technology assumes an essential role in appropriated generation and in joining of renewable energy sources into the electrical grid, and it is broadly utilized and rapidly extending as these applications turn out to be more integrated with the grid- based systems. Amid the most recent couple of years, power electronics has experienced a quick advancement, which is fundamentally because of two components.

1. OVERVIEW

A vigorous power stream calculation which depends on disturbance dismissal control calculation is given in [1]. These methods given in [2] can freely disseminate P and Q double frequency motions. Notwithstanding, the shape and greatness of non-sinusoidal infused currents very build current sounds in the system, which restricts the viability of these methods. Three stage four leg inverters can create sinusoidal voltage waveform in an extensive variety of nonlinear working conditions for more delicate burdens, for example, information exchange and military purposes, since they additionally can issue power quality necessities [3]. In any case, extra stage leg and inductance convolutes the circuit and diminishes the general proficiency. Grid synchronization is of incredible significance for strong control of GCI, quick and precise estimation of grid voltage parameters is basic to work under grid faults. Diverse PLL calculations are accessible in writing expecting to work under grid voltage issues [4].

The first is the advancement of quick semiconductor switches that are equipped for exchanging rapidly and taking care of high powers. The second factor is the presentation of real-time PC controllers that can execute progressed and complex control algorithms. These components together have prompted the advancement of savvy and grid-accommodating converters. In this research, new patterns in power-electronic technology for the joining of renewable energy sources and energy-stockpiling systems are exhibited. This paper is composed as takes after. We portray the current technology and

future patterns in factor speed wind turbines. Wind energy has been demonstrated to be both technically and monetarily practical.

It is normal that current improvements in gearless energy transmission with power- electronic grid interface will prompt another generation of tranquil, proficient, and practical wind turbines. The consistently diminishing prices for the PV modules prompt the expanding significance of cost decrease of the particular PV converters. Energy stockpiling in an electricity generation and supply system empowers the decoupling of electricity generation from demand. At the end of the day, the electricity that can be created at times of either low-demand low-generation cost or from irregular renewable energy sources is moved in time for discharge at times of high-demand high-generation cost or when no other generation is accessible.

WIND TURBINE TECHNOLOGY

Wind energy has matured to a level of development where it is ready to become a generally accepted utility generation technology. Wind-turbine technology has undergone a dramatic transformation during the last 15 years, developing from a fringe science in the 1970s to the wind turbine of the 2000s using the latest in power electronics, aerodynamics, and mechanical drive train designs [5]. In the last five years, the world wind-turbine market has been growing at over 30% a year, and wind power is playing an increasingly important role in electricity generation, especially in countries such as Germany and Spain. The legislation in both countries favours the continuing growth of installed capacity.

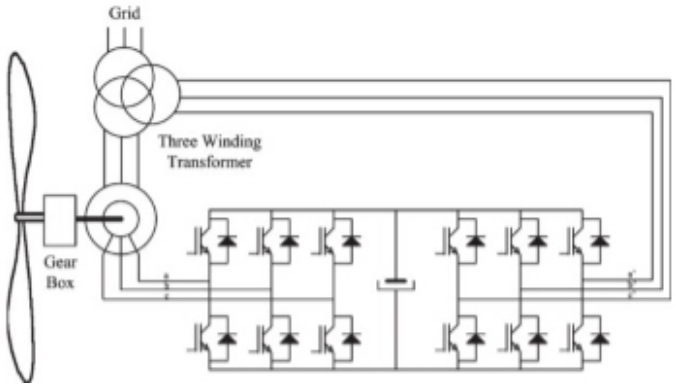

Figure 1 Single Doubly Fed Induction Machine with Two Fully Controlled AC– DC Power Converters

Wind power is very unique in relation to the traditional electricity generation with synchronous generators. Further, there are contrasts between the diverse wind-turbine plans accessible available. These distinctions are reflected in the communication of wind turbines with the electrical power

system. A comprehension of this is, in this manner, basic for anybody associated with the coordination of wind power into the power system. Besides, another technology has been produced in the wind power advertise presenting variable- speed working conditions relying upon the wind speed keeping in mind the end goal to upgrade the energy caught from the wind.

2. CURRENT WIND POWER TECHNOLOGY

Variable-speed wind turbines have progressed dramatically in recent years. Variable-speed operation can only be achieved by decoupling the electrical grid frequency and mechanical rotor frequency. To this end, power-electronic converters are used, such as aac - dc - ac converter combined with advanced control systems.

1. Variable-Speed Concept Utilizing Doubly Fed Induction Generator (DFIG): In a variable-speed turbine with DFIG, the converter feeds the rotor winding, while the stator winding is connected directly to the grid. This converter, thus decoupling mechanical and electrical frequencies and making variable-speed operation possible, can vary the electrical rotor frequency. This turbine cannot operate in the full range from zero to the rated speed, but the speed range is quite sufficient.

2. Variable-Speed Concept Utilizing Full-Power Converter: In this concept, the generator is completely decoupled from the grid [6]. The energy from the generator is rectified to a dc link and after is converted to suitable ac energy for the grid. The majority of these wind turbines are equipped with a multipole synchronous generator, although it is quite possible (but rather rare) to use an induction generator and a gearbox. There are several benefits of removing the gearbox: reduced losses, lower costs due to the elimination of this expensive components, and increased reliability due to the elimination of rotating mechanical components. Enercon supplies such technology.

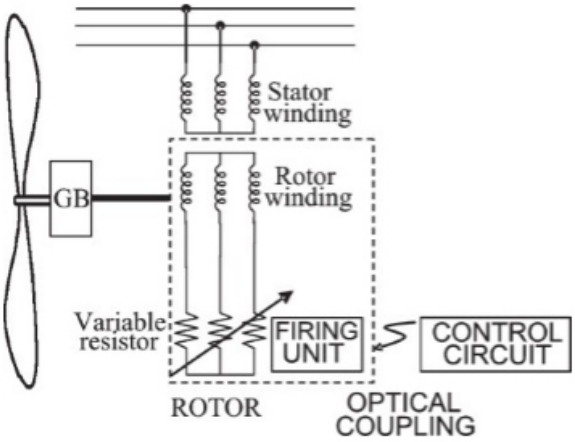

Figure2 Single Doubly Fed Induction Machine Controlled With Slip Power Dissipation inan Internal Resistor

Figure2 shows the plan of a full power converter for a wind turbine. The machine- side three-phase converter fills in as a driver controlling the torque generator, utilizing a vector control strategy.

Semiconductor-Device Technology: Improvements in the performance and dependability of power-electronic variable frequency drives for wind-turbine applications have been directly identified with the accessibility of power semiconductor devices with better electrical qualities and lower prices in light of the fact that the gadget performance decides the size, weight, and cost of the whole power electronics utilized as interfaces in wind turbines.

Recently, the integrated gated control thyristor (IGCT) has been produced as a mechanical incorporation of a GTO in addition to a fragile hard drive circuit that transforms the GTO into a modern high- performance segments with an expansive safe operation area (SOA), lower exchanging misfortunes, and a short storage time.

2.1 Grid-Connection Standards

Voltage Fault Ride-Through Capability of Wind Turbines: As the wind limit expands, network administrators need to guarantee that purchaser power quality isn't imperilled. To empower a substantial scale utilization of the wind energy without trading off the power-system strength, the turbines should remain connected and add to the grid in the event of a disturbance, for example, a voltage dip.

Power-Quality Requirements for Grid- Connected Wind Turbines: The grid collaboration and grid effect of wind turbines have been centredon amid a previous couple of years. The purpose of this intrigue is that wind turbines are among the utilities thought to be potential sources of awful power quality. Estimations demonstrate that the power-quality effect of wind turbines has been enhanced in recent years.

Grid gets to technology as high-voltage dc (HVDC) can associate the wind-cultivate parks to the grid and transmit the power safely and productively to the load focuses. Taking a gander at the general system of financial matters, HVDC transmission systems are most aggressive at transmission separates more than 100 km or power levels of between around 200 and 900 MW. The HVDC transmission offers numerous points of interest over HVAC.

1. Sending and receiving end frequencies are independent.
2. Transmission distance using dc is not affected by cable charging current.

3. Offshore installation is isolated from mainland disturbances and vice versa.
4. Power flow is fully defined and controllable.
5. Cable power losses are low.
6. Power-transmission capability per cable is higher.

3. DIRECT-DRIVE TECHNOLOGY FOR WIND TURBINES

Direct-drive applications are on increase because the gearbox can be eliminated. As compared to a conventional gearbox- coupled wind turbine generator, a direct- drive generator has reduced the overall size, has lower installation and maintenance cost, has a flexible control method and quick response to wind fluctuations, and load variation. For small wind turbine, permanent magnet synchronous machines are more popular because of their higher efficiency, high-power density, and robust rotor structure as compared to induction and synchronous machines.

4. TECHNICAL ISSUES FOR GRID CONNECTED RENEWABLE ENERGY SOURCES

Renewable energy in recent years become more and more common, due to the large increase in generation from renewable energy sources such as small hydropower stations, wind turbines, photovoltaic (PV) etc.

5. TECHNIQUES FOR POWER QUALITY IMPROVEMENT

Resistors, capacitors, and inductors all consume power once a current goes through them, and unequipped for power pick up. Consequently, any RLC filter might be a passive filter, especially with the inductors encased. Another real normal for the passive filters is that the filters don't might want to relate outer power supply for operation. Passive filters additionally make a little measure of clamour, because of the warm commotion in the components. A few disadvantages for passive filters can filter just the frequencies Resonances will happen to owe to the collaboration between the passive filters and different loads, with erratic outcomes. To leave these drawbacks, recent endeavours are concentrated in the advancement of active filters. Filters with parts like operational enhancers, transistors, or alternative active parts are alluded to as active filters. They utilize capacitors and resistors, anyway not inductors.

6. NEW ENERGY POWER GRID- INTEGRATION ON GRID POWER ELECTRONICS

With the development of science and technology and the national economy, electricity is an important resource for people's lives. The coal, oil and other fossil fuel bear 90% of the traditional power load. Entering the new century, we should pay attention to energy and environmental issues. On the one hand, with the start of the industrial revolution, the consumption of traditional energy sources rapid

increases and traditional energy is non-renewable resources. Excessive development and using will eventually lead to depletion of resource. On the other hand, a large number of traditional energy which use makes ecological deterioration. Especially the emissions of carbon dioxide cause the greenhouse effect.

7. IMPACT OF DISTRIBUTED POWER FOR POWER QUALITY

The system of distributed generation was included in the distribution system. It is a fundamental pattern for the improvement of distributed power generation. In any case, with the penetration of DG in power systems expanding, it has an impact on the power system, including the power system power quality, load anticipating, system arranging, system flow, system failure and security devices. This area will consider the effect of power quality, and break down the deviation of the voltage and harmonic for power quality. The distinguished power level of the transport will be not exactly without getting to distributed power. In light of this data, the system transport side voltage is set lower than the genuine needs of the client, and this will make the voltage of part of the client is below a specific standard.

8. CONCLUSION

This paper gives the report on two forms of renewable energy wind and solar energy, and on the role of smart grids in addressing the problems associated with the efficient and reliable delivery and use of electricity and with the integration of renewable sources. In this research different power quality issues are addressed and a FACTS device STATIC COMPENSATOR (STATCOM) is connected at a point of common coupling for grid connected wind turbine to reduce the power quality problems like harmonics in the grid current, by injecting superior reactive power in to the grid of wind turbine.

And also an active power filter implemented with a four leg voltage-source inverter using DQ (Synchronous Reference Frame) based Current Reference Generator scheme is presented for renewable based distributed generation system of PV cell. As the world's electricity demand increases, more environmental constraints is given to conventional energy sources such as fossil or nuclear energy.

The power quality issues of wind power grid include technical problems and administrative difficulties of the power grid in our nation. Accordingly, the search subjects about the wind cultivate power quality appraisal and control measure sown imperative hypothetical and common sense centrality. The unbalanced loads or DGs connected in MG will interactive with ESS inverter, which would debase the voltage control performance of inverter and prompts MG voltage to unbalance. In this research, a novel UTVCS given negative-arrangement compensation is proposed. Rather than the ordinary control

strategy, with the proposed UTVCS, both the inverter control and the operation mode of MG are considered, subsequently the method in this research has focal points in enhancing the MG power quality, and it is essentially realized.

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An Investigation of Delay Estimation Model for Effective High Spped VLSI

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A B S T R A C T

In this paper a closed shape matrix rational model for the calculation of step and limited incline reactions of Resistance Inductance Capacitance (RLC) interconnects in VLSI circuits is displayed. This model permits the numerical estimation of deferral and overshoot in loss VLSI interconnects. The proposed technique depends on the U-change, which gives rational capacity approximation to getting inactive interconnect model. With the decreased request loss interconnect exchange capacity, step and limited slope reactions are acquired and line deferral and flag overshoot are assessed. The assessed deferral and overshoot qualities are contrasted and the Euder strategy, Pade technique and HSPICE W-component model. The half postpone results are in good agreement with those of HSPICE inside 0.5% mistake while the overshoot blunder is inside 1% for a 2 mm long interconnect. For global lines of length more than 5 mm in SOC (framework on chip) applications, the proposed technique is observed to be almost four times more exact than existing methods.

Keywords – Delay; matrix rational model; ramp input; RLC interconnects; transient analysis; transfer function; U-approximation

1. INTRODUCTION

As the physical dimensions in VLSI technologies downsize, interconnect delay rules the entryway delay in deciding circuit execution [1]. In profound submicron VLSI circuits it is important to have computationally economical and exact interconnect postpone models. In this way for the plan of complex circuits, more precise explanatory models are expected to foresee the interconnect delay precisely.

Initially VLSI interconnects were modeled as RC lines and single post Elmore-based models [2]– [3] on account of long channel gadget postpone predominance over unimportant interconnect delay. However for rapid interconnects, inductance impacts are ending up plainly dynamically imperative and can never again be disregarded. Under these conditions, the Elmore model comes up short since it doesn't consider the inductance impacts [4]. It is important to utilize a moment arrange model, which incorporates the impact of inductance. Kahng et al. considered proportional Elmore defer model in view of the Resistance Inductance and Capacitance (RLC) of the interconnects [4] and [5]. Ismail et al. [6] proposed two shaft model to catch far end time domain answer for single line interconnect.

A disentangled voltage exchange work acquired utilizing Taylor arrangement approximation for transient analysis [7]-[8] has less exactness in postpone calculation. Nakhla et al.[9] utilize changed nodal analysis (MNA) for obtaining far end and close end reactions of interconnects. Roy [10] augmented [9] for obtaining more exact far end reactions of coupled RLC interconnects utilizing defer arithmetical equations.

A lattice rational-approximation model for SPICE analysis of fast interconnects is introduced in [11]-[12], be that as it may, the approximations made to determine the models

$$\text{Where}\emptyset = \begin{matrix} 0 & -Z \\ -Y & 0 \end{matrix}$$

added to error. This has been augmented utilizing Pade approximation model [13] to gauge the postponement of interconnects. All the above models still experience the ill effects of different errors and need change for precise defer estimations.

2. ANALYSIS OF RLC INTERCONNECT

The solution of interconnects are described by telegrapher's equations as

$$\frac{\partial}{\partial x} V\ z, s = -\ R + sL\ I\ z, s$$

$$\frac{\partial}{\partial x} I\ z, s = -sCV\ z, s$$

where "s" is the Laplace-change variable, z is a variable which speaks to position; V(z,s) and I(z,s) remain for the voltage and current vectors of the transmission line, individually, in the frequency domain; and R, L and C are the per unit length (p.u.l.) resistance, inductance, and capacitance matrices, separately.

The solution of (1) can be written as an exponential matrix function as

$$\begin{matrix} V\ d, s \\ -I\ d, s \end{matrix} = e^{\emptyset d} \begin{matrix} V\ 0, s \\ I\ 0, s \end{matrix}$$

and 'd' is the length of the transmission line, with Z=R+sL and Y=sC. The exponential matrix of (2) can be written in terms of cosh and sinh functions as

$$e^{\emptyset d} = \begin{matrix} \cosh\ d\ \sqrt{ZY} & -Y^{-1} \sinh d\ \sqrt{ZY} \\ -Y_0 \sinh\ d\ \sqrt{ZY} & \cosh d\ \sqrt{YZ} \end{matrix}$$

Where

$$Y_0 = Y \quad \overline{YZ}^{-1}$$

3. PROPOSED U MODEL

This model is based on a generalized U- transform [14]. For the power series expansion of a function f(x), where 'x' is a complex variable

$$f\ x = a_n \sum_{n=0}^{\infty} x^n$$

The sequence $\{s_n\}$ is a partial sum of original series

$$S_n = \sum_{k=0}^{n-1} a_k x^k$$

The closed form rational function approximation for an exponential matrix is

$$u_{kn}\ S_n = \frac{\sum_{j=0}^{n+k-1} x^{i\,k} \sum_{j=0} w_{knj} a_{j-1}}{\sum_{j=0}^{k} w_{knj} x^i}$$

Where

$$w_{knj} = -1\ ^j \frac{k!}{j!\ k-j\ !} \frac{n+k-j\ ^{k-2}}{a_{n+k-j-1}}$$

Thus uknrepresents a table of rational functions, every component of which is gotten from n + k terms of the first grouping {Sn, n = 1, 2...} and is an approximant of the function f(x) determined previously. Calculation system for evaluating postponement and overshoot utilizing U- approximants are as per the following.

1. Use the Interconnect line parameters according to Table I.
2. Telegrapher's equations are tackled and the arrangement can be composed as exponential network.
3. This transfer function network parameters can be approximated utilizing the U-model.
4. In the proposed model compute the coefficient of the exponential function i.e., where

$$0 \leq i \leq n$$

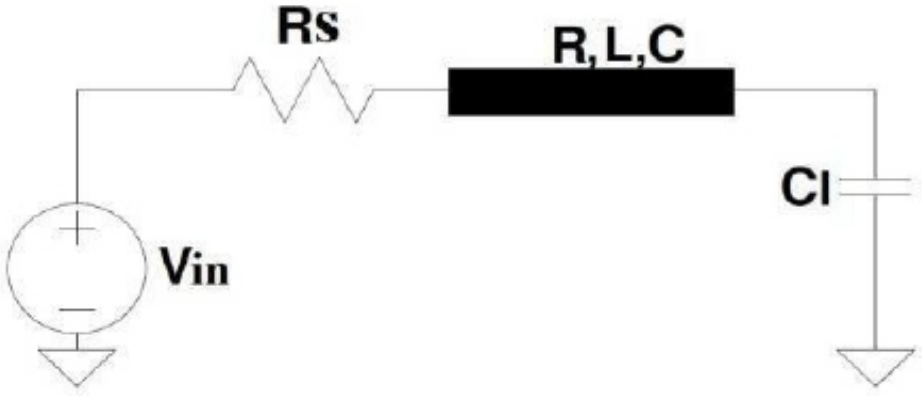
5. Calculate wknj from the connection (4)
6. Calculate the internal whole of the Eq (3) numerator.
7. Total of the numerator is gotten
8. Calculate the aggregate total of the denominator of the U-approximants
9. Calculate the U-approximants.
10. Make utilization of the U-approximants to get approximated transfer function

11. Find the time domain response of approximated transfer function utilizing backwards Laplace transform to estimate delay and overshoot of interconnect.

The fundamental thought of the grid rational- approximation model is to utilize foreordained coefficients to analytically get rational functions for (2). To get an inactive model, the exponential function eϕd is approximated utilizing Eq (3) and the resultant model is utilized for obtaining time response.

A solitary RLC line is appeared in Fig. 1 The line is driven by a stage info and 1-V limited ramp with rise time of 0.1 ns. This speaks to an indicate point interconnection driven by a transistor (modeled as a resistance Rs) and connected to the following entryway (modeled as a capacitance Cl).

Fig. 1 Circuit model of the single-line



distributed RLC interconnect

The frequency-domain solution at the far end is expressedas

$$\frac{V_f}{} = \frac{V_{in}}{1 + sR_sc_1 \cosh \Gamma d + R_sc_0 + sC_1y^{-1} \sinh \Gamma d}$$

Where

$$\Gamma = \overline{YZ},$$

Rs are the source resistance at the close end, Cl is the heap capacitance at the far end, and Vin is the information voltage. The correct transfer function of dispersed RLC transmission line has cosh and sinh terms, which are increased with Yo and it's inverse. It is to a great degree hard to discover the time domain response of this complex transfer function, so a few approximations are proposed in writing to discover the time domain response. An approximate transfer function has been inferred utilizing U

change. This transfer function is inverse Laplace changed to get time domain response for estimation of postponement and overshoot in single RLC interconnect.

4. SIMULATION RESULTS

The single RLC line is displayed in this area to show the legitimacy and proficiency of the proposed method. The outcomes were acquired utilizing MATLAB R2010a working on HP 64-bit Intel i5 processor with clock speed of 2.53 GHz and are additionally contrasted and HSPICE utilizing the W-element method.

The common interconnect parameters [16] considered for reproduction of single RLC interconnect are given in table-I. The Pade approximation, Eudes model and proposed U- approximation are executed in MATLAB for a similar arrangement of info parameters and different approximation orders.

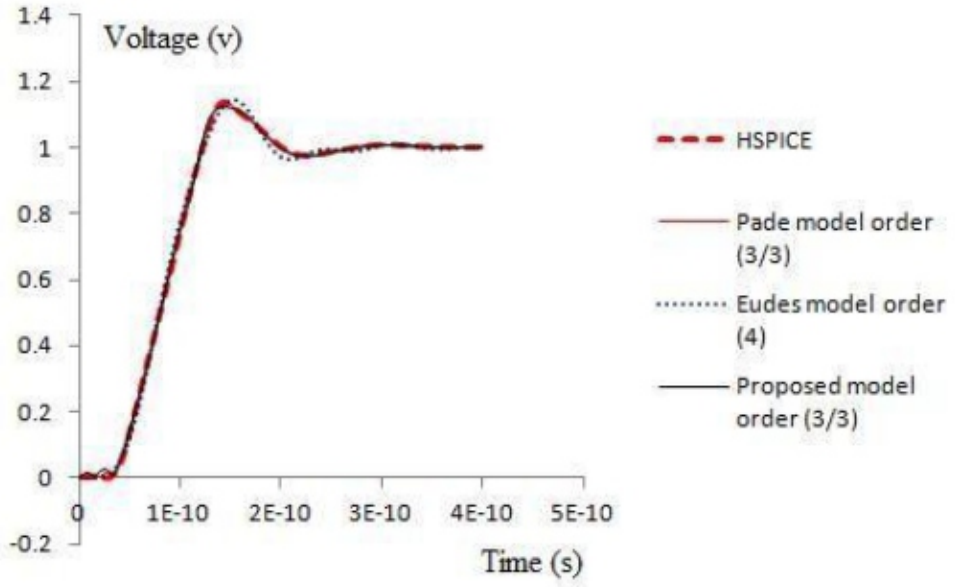
Table I: The values of Interconnects parameters

Vdd	1v
Length	0.2cm
Resistance	88.29Ω/cm
Capacitance	1.8pF/cm
Inductance	15.38nH/cm
Load capacitance	0.05fF to 0.1fF
Source resistance	20Ω to 100Ω
Input ramp rise time	0.1ns

The accuracy of proposed model approved utilizing the frequency response of cosh function as appeared in Fig. 2. The frequency response is gotten utilizing pade (3/3) and proposed U-model (3/3) are contrasted and the correct arrangement of telegrapher's equations. It is observed that, the proposed method is superior to Pade method and well matches with correct cosh function for the order of 3/3 up to the frequency of 25 Ghz.

From Fig. 3, it is seen that, the proposed U- approximation and Pade method are close when contrasted with HSPICE. In any case, Eudes model of order 4 has more overshoot when contrasted with different methods.

Fig: 2.Transient analysis of single interconnect line, when length =0.2cm, Rs=50Ω and Cl=50fF.



The MATLAB result of step response and limited ramp response are plotted for the line length of 0.2 cm, source resistance of 100ω and load capacitance of 100fF. Step response in Fig. 4 has less ringing in proposed method when contrasted with Pade method, for a similar approximation order of 3/3, though Fig. 5 gives limited ramp response of single line interconnect utilizing U-model matches extremely well with the HSPICE. Be that as it may, Eudes model needs all the more settling time when compared with the proposed model

Fig: 3.Step response of single line when length =0.2cm, Rs=100Ω and Cl=100fF.

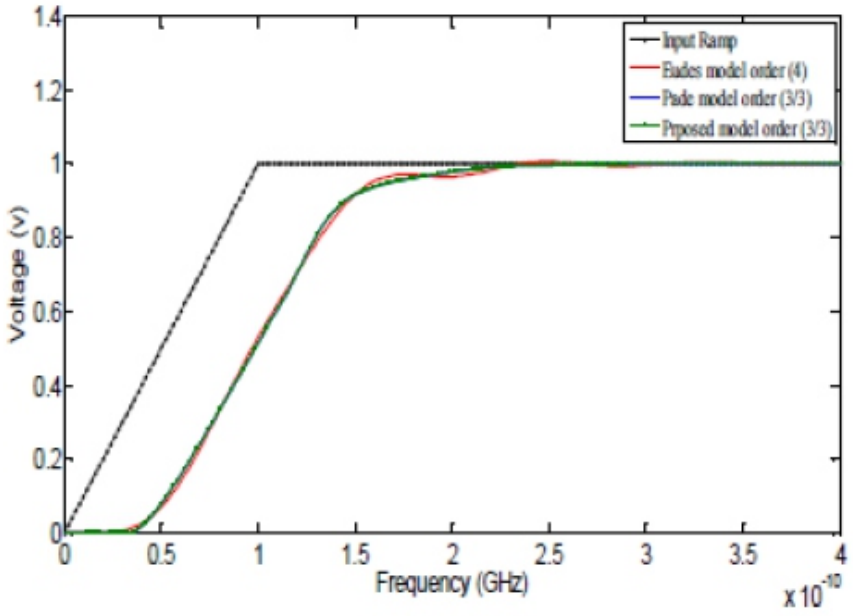


Fig: 4.Ramp response of single line when length =0.2cm, Rs=100Ω, Cl=100fF.

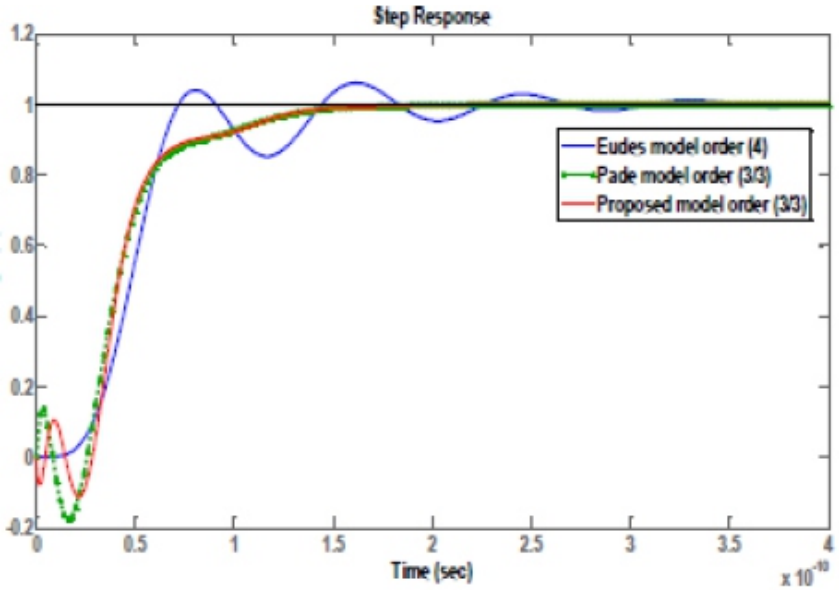


Table II: Comparisons of 50% delay of HSPICE W Element, Eudes model Pade model and proposed model for various lengths source Resistances and load Capacitances.

L (cm)	Rs (?)	Cl (fF)	HSPICE 50% delay (ps)	Eudes model order (4) 50% delay (ps) (%Error)	Pade Order 3/3 50% delay (ps) (%Error)	Proposed Model order (3/3) 50% delay (ps) (%Error)
0.2	50	50	79.8	79.1 (0.8%)	80.2 (0.5%)	80.2 (0.5%))
	100	100	98.7	96.8 (1.92%)	98.6 (.1%)	98.65 (0.05%)
0.5	50	50	135.7	142.8 (5.23%)	137.8 (1.54%)	137.7 (1.4%)
	100	100	156.6	162.6 (3.83%)	151.9 (3%)	155.3 (0.83%)
1	50	50	231.2	250.2 (8.21%)	211.1 (8.69%)	224.7 (2.811%)
	100	100	255.6	284.8 (11.42%)	249.7 (2.3%)	252.5 (1.21%)

Table III: Comparisons of overshoot of HSPICE W Element, Eudes model, Pade model and proposed model for various lengths, source Resistances and load Capacitances.

L (cm)	Rs (?)	Cl (fF)	HSPICE Overshoot (V)	Eudes model order (4) Overshoot (V) (%Error)	Pade Order 3/3 Overshoot (V) (%Error)	Proposed Model order (3/3) Overshoot (V) (%Error)
0.2	50	50	1.14	1.14 (0%)	1.12 (1.7%)	1.13 (0.87%)
	100	100	1.00	1.00 (0%)	1.00 (0%)	1.00 (0%)
0.5	50	50	1.15	1.24 (7.8%)	1.15 (0%)	1.14(0.87%)
	100	100	1.00	1.03 (3%)	1.00 (0%)	1.00 (0%)
1.0	50	50	1.00	1.09 (9%)	1.02 (2%)	1.01 (1%)
	100	100	1.00	1.00 (0%)	1.00 (0%)	1.00 (0%)

The Tables II and III give the comparisons of 50% delay and overshoot values acquired utilizing HSPICE for different lengths, source Resistances and load Capacitances. These tables incorporate the percentage error values as for HSPICE. From Table II the Eudes model of order 4 has most pessimistic scenario error of 11.42%, while Pade and proposed models have 8.69% and 2.811%.

It can be observed that the methods executed for global lines have more error percentage than our proposed method. Both Pade and proposed methods perform correspondingly for littler length interconnects while Eudes method has more error percentage.

As saw in Table III, the Eudes model has most pessimistic scenario overshoot error percentage of 9%, however Pade model has an error percentage up to 2% while the proposed model has error inside 1%. On account of overshoot estimation our model is best for all cases. For 2 mm run lines theproposed method has delay and overshoots errors inside 1%.

5. CONCLUSION

This paper exhibits a U-transform based shut frame model for delay and overshoot estimation of fast VLSI interconnects in DSM administration. A solitary line interconnect has been utilized for approving the proposed model by contrasting and the Eudes model, Pade method and HSPICE. In SOC (framework on chip) applications, for global lines of lengths 2 mm or more the proposed method is observed to be more accurate than existing methods. This method can be utilized to gauge the flag trustworthiness qualities of Carbon nano tubes.

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Plan and Assessment of FinFET based SRAM Cells at 22nm and 14nm Node Technologies

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ABSTRACT

In this paper are situation more than 85-90% of the chip territory is for the most part involved by memory.

There is a requirement for quicker and solid memory framework for different incorporated gadgets from PCs to different handheld gadgets. The memory gadgets, for example, SRAM, DRAM and so on were served by the customary MOSFETs till to date however as the interest of the better performing and the reduced displaying of the incorporated gadgets are causing the disappointment of MOSFETs activities. The MOSFET scaling is endured by Short Channel Effects (SCE's).SRAM is one of the memories mainly utilized in the store memory of gadgets. It must be quicker, less power devouring and dependable however this is influenced by CMOS scaling causing process varieties. Here in this paper the substitute answer for the issues looked by MOSFET based SRAM is overwhelmed by FinFET based SRAM. A 6T short gated FinFET based SRAM is taken for the investigation and the flavor models are made at 22nm and 14nm utilizing Predictive Technology Models (PTM) and reenacted utilizing HSPICE. The execution is broke down as far as Static Noise Margin (SNM), power and deferral for the 6T SRAM. The outcomes demonstrates FinFET based SRAM is quicker, solid and the power utilization is fundamentally diminished and offers great exchange offs at lower innovation hubs.

Keywords: FinFET, SRAM Cell, CMOS, SNM, PTM Read delay, Write delay.

1. INTRODUCTION

As of late, the interest for low power gadgets has been increments massively because of quick development of battery worked compact applications, for example, PDAs, mobile phones, workstations and other handheld gadgets. Be that as it may, restrictions of persistent innovation scaling have as of late made power decrease an essential plan issue for the advanced circuits and applications. As MOS transistors enter profound submicron sizes, bothersome results with respect to control utilization emerge. Up to this point, dynamic or exchanging power segment ruled the all out power scattered by an IC. Voltage scaling is the best strategy to diminish dynamic power because of the square law reliance of computerized circuit dynamic power on the supply voltage. Thus, this requests a decrease of edge voltage to look after execution. Low edge voltage results in an exponential increment in the sub-limit spillage current. Then again as innovation downsizes, shorter direct lengths result in

expanded sub-edge spillage current through an off transistor. Along these lines, in DSM process static or spillage control turns into an extensive extent of the complete power scattering. Along these lines door length scaling expands the gadget spillage exponentially crosswise over innovation ages. Besides, the cell strength will keep on corrupting with diminishing the framework supply voltage (VDD) and the transistor limit voltages (VT) in nanometer innovation hubs.

The FinFET transistor structure has been acquainted as an option with the mass Si MOSFET structure for enhanced versatility. The structure has two doors which can be electrically detached and have two distinct voltages (back entryway) for an enhanced task. In the twofold door (DG) working mode, the two entryways have associated together to switch the FinFET on/off, while in the back-door (BG) working mode, they are one-sided autonomously – with one entryway used to switch the FinFET on/off and the other door used to decide the edge voltage.

Difficulties in the kept scaling of planar mass CMOS gadgets incorporate overwhelming corona doping to adjust for debased short channel impacts, diminished transporter mobilities in the channel, expanded source-deplete spillage current, arbitrary dopant changes, and basic measurement control. FinFETs are potential choices to mass FETs because of their more grounded electrostatic command over the divert bringing about enhanced short channel conduct. These gadget qualities make FinFETs a useful for SRAM applications.

2. FINFET TECHNOLOGY & DESIGN PARAMETERS

The FINFET based transistors offers great tradeoff for power also offering fascinating deferral. The Figure 2.1 demonstrates the 3D structure of multi-FIN based field impact transistors. Fig 1 demonstrates a basic structure of FinFET, it is a 4 terminal gadget including source and deplete associated by a channel, the channel is folded over by numerous doors, for this situation we consider 2 entryways to be specific forward and in reverse entryways or front and back entryways. A FinFET resembles a FET, however the channel has been "turned on its edge" and made to stand up subsequently structure gave the name for the gadget as FinFET. FinFETs might be substituted into a previous mass CMOS structure by only shorting the front-and back- entryways together amid gadget manufacture to permit just a single door association for every FinFET. This transistor setup is frequently called shorted entryway (SG).

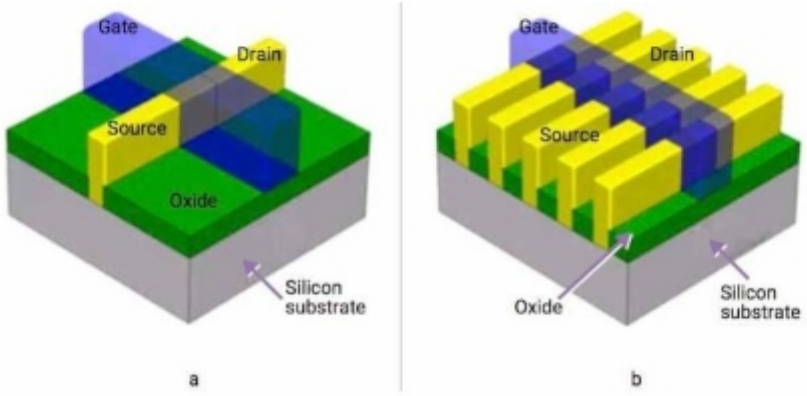

Fig.1.3D Multi-FIN Based Field Effect Transistor Structure

The gadget parameters contemplations are one of the imperative strides in building up a flavor model and after that reproducing it. Regularly utilized FinFET recreation models accessible to the examination network are the Predictive Technology Model (PTM) [7] and BSIM- CMG/BSIM-IMG [8]. Table1 demonstrates the estimations of FinFET parameters utilized in this work. The estimations of the parameters appeared table 1 are considered concerning PTM.

Table.1 Design considerations

PARAMETER	22nm FinFET	14nm FinFET
Gate Length (Lg)	22nm	14nm
Supply Voltage	0.9v	0.8v
Thickness of Fin (tfin)	10nm	10nm
Height of Fin (Hfin)	30nm	23nm
Thickness of oxide (tox)	1.4nm	1.3nm

The gadget parameters referenced here are vital in structuring any circuit utilizing FinFET. Advancements hubs are characterized dependent on the entryway length, as the gadget is downsized the supply voltage, oxide thickness and tallness of the balance is likewise downsized to meet the necessities and to maintain a strategic distance from the scaling issue, for example, speed immersion. The plan contemplations are absolutely done on the geometric portrayal of FinFET gadget structure [13-15]. There will be a great deal of varieties in changing the estimations of any of these parameters referenced. In our investigation we have concentrated on these 5 parameters referenced in the table.

3. SRAM CELL PERFORMANCEOPERATION

3.1. Static Noise Margin: Static Noise Margin (SNM) is a standout amongst the most vital measurement for SRAM memory cell. SNM influences both read and compose edge, which is identified with the limit voltages of the NMOS and PMOS gadgets of the SRAM cell. The SNM is

characterized the base clamor voltage present at every one of the cell stockpiling hubs important to flip the condition of the cell. SNM parameter can be better comprehended by illustration the inverter attributes and afterward reflecting it on itself and estimating the greatest square between them. For soundness of the SRAM cell, great SNM is required that relies upon the estimation of the cell proportion, pull up proportion and furthermore supply voltage. Driver transistor is in charge of 70 % estimation of the SNM. Cell proportion is the proportion between sizes of the driver transistor to the heap transistor amid the read activity. Draw up proportion is likewise only a proportion between sizes of the heap transistor to the entrance transistor amid composes activity.

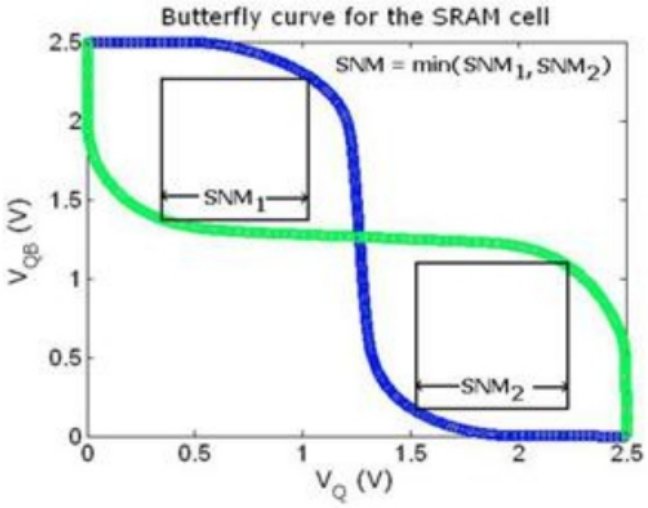

Fig.2. SRAM butterfly curve

Cell Ratio = (W1/L1)/ (W5/L5) – During Read task Pull up Ratio = (W4/L4)/ (W6/L6) – During Write activity SNM, influences both read and compose edges that are specifically identified with the edge voltages of NMOS and PMOS gadgets. To increment SNM, we can build the edge voltages of PMOS and NMOS in any case, that expansion is constrained and Likewise having a limit voltage that is exceptionally high makes the gadgets hard to work as it turns out to be difficult to flip the MOSFET. Subsequently we swing to the utilization of FinFETs for upgrade of measurements that will improve SRAM execution. In our examination we have determined SNM at reserve method of the FinFET based 6T SRAM cell utilizing graphical strategy by recreating the FinFET SRAM zest show in HSPICE. SNM ought to be high for a gadget to perform easily and create legitimate yields.

3.2. Power: Power utilization and dissemination is one of the real execution metric of SRAM. The MOSFET based SRAM neglects to work when it is downsized to the nanometer routine of innovation hub, causing high power utilization and dissemination of the SRAM cell. The power devoured by the FinFET based SRAM cell at 22nm and 14nm innovation hubs are examined here. The framework exchange offs of intensity are likewise seen here. The power utilization regularly identifies with the

supply voltage and subsequently as we downsize the FinFET, the power utilization of the whole circuit should likewise diminish however in few cases the dissemination of intensity may expand on account of the thickness of the incorporated gadget. Thus understanding the measurement control is essential here.

3.3. Delay: The delay of the SRAM cell can be estimated as far as the compose and read postponement of the circuit. The compose delay is the time taken by the SRAM circuit to compose a touch of information into the memory i.e. the hook circuit. The read postponement is the time taken for extricating the put away piece of information from the hook to yield. The read deferral additionally relies on the sense intensifier hardware utilized for perusing the yield, in the event that the detecting is quick, getting the yields will be likewise quick. The compose and read postponements are gotten for FinFET based SRAM cell at 22nm and 14nm hub advancements. Again the framework exchange offs between powers, territory and deferral are contemplated here.

4. SRAM MEMORY

4.1. Static Random Access (Memory [SRAM] Cell): It is a standout amongst the most usually utilized sort of semiconductor memory that utilizes a bi-stable hooking hardware to store each piece, it is static in nature and not the same as D-RAM which is dynamic and is invigorated occasionally. SRAM is unpredictable and will lose its information in the event that it isn't controlled. It is utilized in PCs, workstations and other fringe gear alike inner CPU reserves, hard circle cradles and so forth.

There are two sorts of SRAM cells:

1. Asynchronous SRAM
2. Nonvolatile SRAM

SRAMs are additionally characterized based on the transistor type used to assemble a SRAM. BJTs are quick however expending a great deal of intensity, at that point came the MOSFET bases SRAMs which supplanted the BJTs and served every one of the tasks with higher execution. The need of better execution and downsizing the measure of MOSFET with diminished short channel impacts made ready for the possibility of FinFET based SRAMs. The FinFET based 6T SRAM circuit is appeared in taking a gander at the circuit charts we can plainly comprehend the nearness of twofold entryways specifically forward and in reverse doors in the FinFET based SRAM cell. In our examination we have considered the twofold entryway short gated FinFET SRAM cell where the forward and in reverse door are shorted and furnished with the door input. This gives better channel control and the disappointment of MOSFET at nanometer routine innovation hub can be survived.

4.2. FinFET based SRAM Cell: The information stockpiling cell, i.e., the 1-bit memory cell in static RAM exhibits, perpetually comprises of a basic hook circuit with two stable working focuses (states). Contingent upon the safeguarded condition of the two-inverter hook circuit, the information being held in the memory cell will be translated either as a rationale "0" or as a rationale "1" .To get to (read and compose) the information contained in the memory cell by means of the bit line, we require somewhere around one switch, which is constrained by the relating word line, i.e., the line address determination flag normally, two corresponding access switches comprising of nMOS pass transistors are executed to associate the 1-bit SRAM cell to the reciprocal piece lines (segments). This can be compared to turning the vehicle guiding wheel with both left and right submits correlative headings.

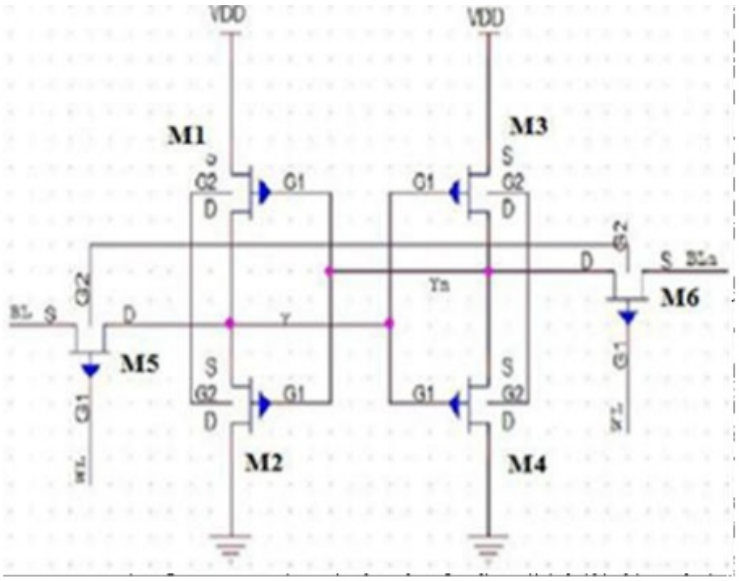

Fig.3.FinFET based 6T SRAM

The circuit structure of the full FinFET static RAM cell is appeared in Figure 3, alongside the pFET segment pull-up transistors on the integral piece lines. The most imperative favorable position of this circuit topology is that the static power dispersal is significantly littler; basically, it is restricted by the spillage current of the pFET transistors. A FinFET memory cell accordingly draws current from the power supply just amid an exchanging progress. The low backup control utilization has positively been a main impetus for the expanding noticeable quality of FinFET SRAMs.

5. RESULTS AND DISCUSSIONS

The spice models of FinFET SRAM are first made for 22nm and are reenacted utilizing HSPICE and the recreation waveforms are seen utilizing the universe adapt. The reenactments waveforms for compose and read postponements are as appeared in Fig 4 and Fig 5 separately at that point the models are altered for 14nm and the procedure is rehashed. Fig. 6 and 7 demonstrates the read and compose activity for the FinFET based 6T SRAM at 14nm. The voltage utilized is 0.8v.

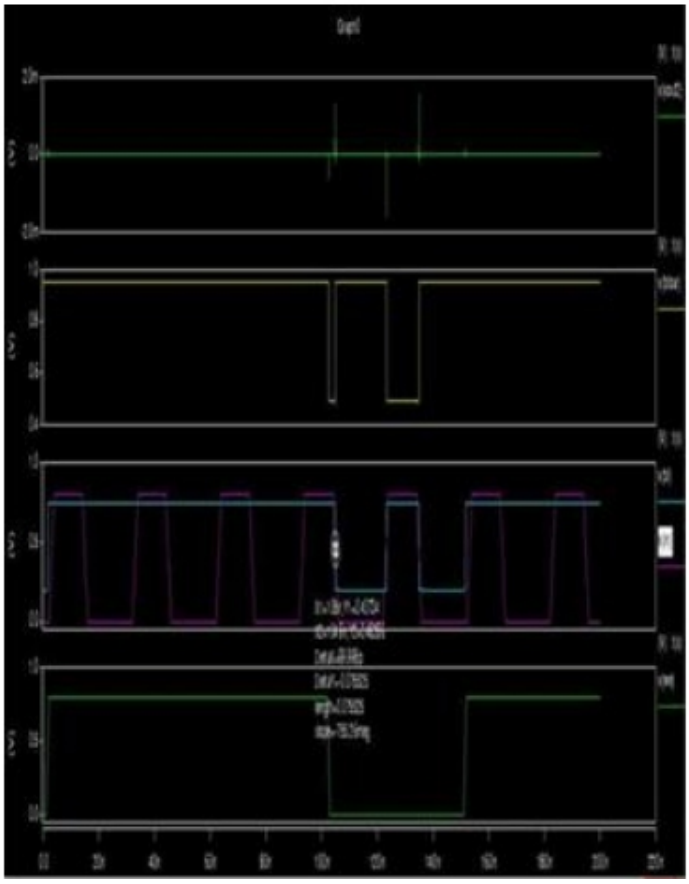

Fig.4. Write delay for 22nm FinFET based SRAM

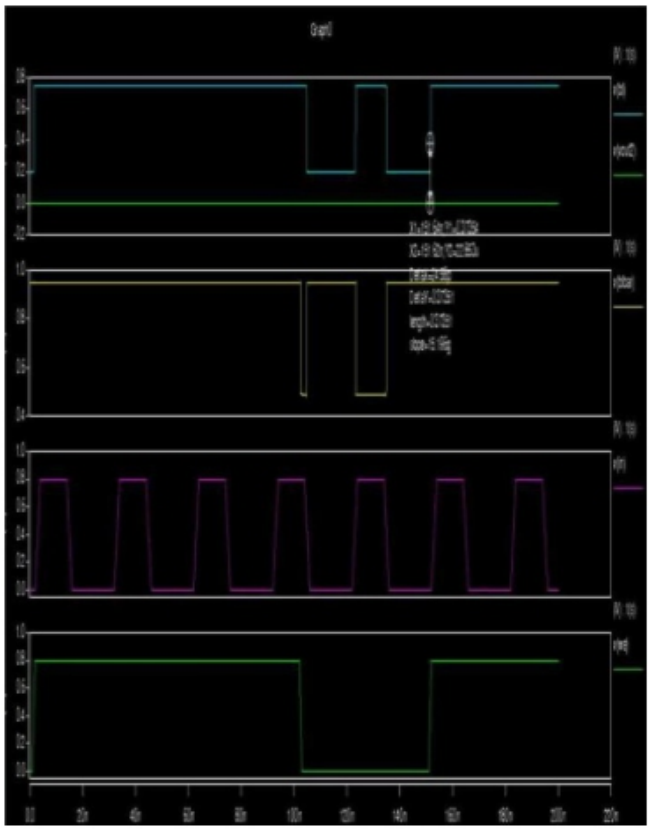

Fig.5. Read delay for 22nm FinFET based SRAM

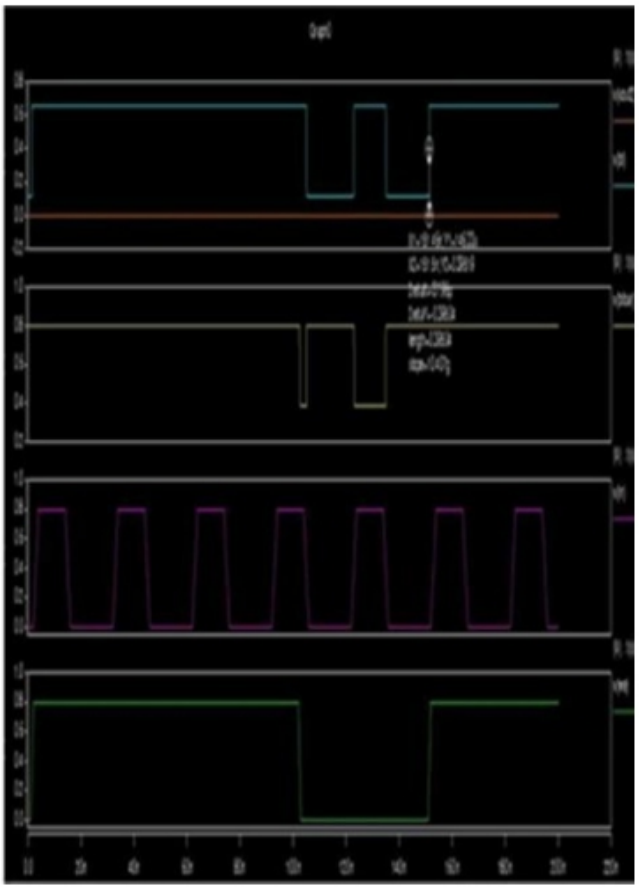

Fig.6. Write delay for 14nm FinFET based SRAM

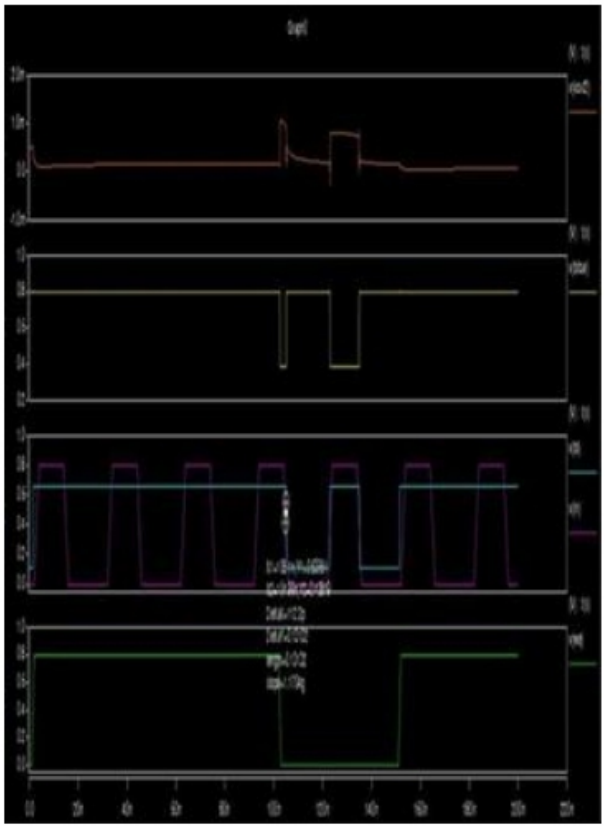

Fig. 7: Read delay for 14nm FinFET based SRAM

Here the word empower (we) goes about as a control flag. At the point when the word empower is low, compose activity is finished. At the point when the word empower is high the information what was composed will be detected by the sense intensifier. The read task is performed when word empower is high Fig. 8 and 9 demonstrates the butterfly bends for FinFET based 6T SRAM cell at 22nm and 14n separately. This demonstrates the Static Noise Margin (SNM) at backup mode esteems got for each situation of the SRAM cell. These butterfly bends are acquired utilizing the graphical strategy plot in HSPICE. The SNM esteems are perused from the DeltaY esteem, considering the fig.8 the DeltaY esteem indicates 0.20738 in volts, henceforth the SNM esteem got for 22nm FinFET 6T SRAM is 207.38 mV. So also considering Fig.9 we can see the DeltaY esteem got is 0.18467 in volts, henceforth the SNM got for 14nm FinFET 6T SRAM cell is 184.67mV.

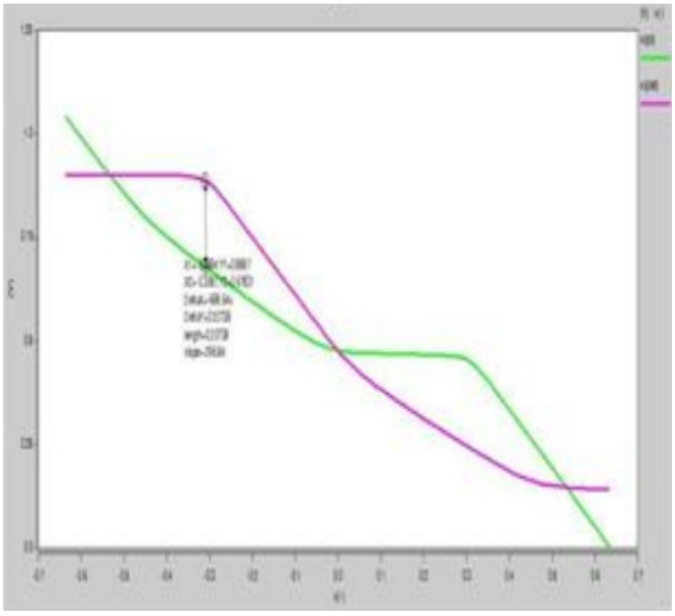

Fig.8.Butterfly curve for FinFET based 6T SRAM at 22nm

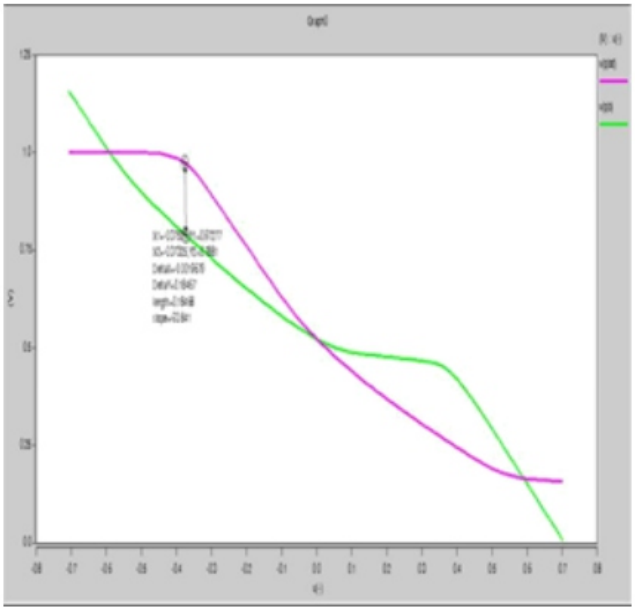

Fig.9: Butterfly curve for FinFET based 6T SRAM at14nm

6. CONCLUSION

The FinFET based 6T SRAM cell at 22nm and 14nm are dissected here. The got outcomes for the SRAM zest models demonstrate a promising answer for MOSFETs scaling issues. The static commotion edge esteems got for the SRAM cell demonstrates that the FinFET based SRAM cell is dependable at lower innovation hubs and the tolerant limit is better at the nanometer routine. The power utilization of the gadget has diminished altogether and this memory cell could be coordinated with any such memory based gadgets requiring less power utilization. The speed of the memory circuits are additionally considered regarding the compose and read defer which demonstrates that the read and compose speed has expanded and the framework exchange offs between power, zone and postpone is sensible where the deferral has expanded at 14nm model yet the power and territory has decreased fundamentally.

7. ACKNOWLEDGEMENTS

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A Study and Analysis of Data on Projects for Clean Development Mechanism

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ABSTRACT

The Clean Development Mechanism (CDM) allows emission-reduction projects in developing countries to earn certified emission reduction (CER) credits, each equivalent to one tonne of Carbon-di-oxide. These CERs can be traded and sold, and used by industrialized countries to meet a part of their emission reduction targets under the Kyoto Protocol.

This paper discusses Kyoto Protocol (KP) as the Background of Clean Development Mechanism (CDM) and also discusses CDM as one of the mechanisms of Kyoto Protocol. The governance mechanism of CDM is also explained. CDM being introduced and developed with the twin objective of sustainable development of the developing countries, and a flexible and cost effective tool for the legally binding GHG mitigation by the developed countries, vital and latest statistics on CDM projects is provided and analysed for scenario building. At the end of the paper a discussion has also been made and conclusions provided. Some future research areas have also been identified.

Keywords: Kyoto Protocol; KP; Clean Development Mechanism; CDM; Sustainable Development, Energy; Environment; Green House Gases; GHG; UNFCCC

1. BACKGROUND OF CDM

The Clean Development Mechanism (CDM) allows emission-reduction projects in developing countries to earn certified emission reduction (CER) credits, each equivalent to one tonne of Carbon-di-oxide. These CERs can be traded and sold, and used by industrialized countries to meet a part of their emission reduction targets under the Kyoto Protocol. The roots of the Clean Development Mechanism (CDM) lie in the Kyoto Protocol. The Kyoto Protocol is generally seen as an important first step towards a truly global emission reduction regime that will stabilize anthropogenic (i.e., human-emitted) Green House Gases (GHG) concentration at a level which will avoid dangerous climate change. The Kyoto Protocol was adopted at the third conference of the Parties (COP 3) to the United Nations Framework Convention on Climate Change (UNFCCC) in Kyoto, Japan, on December 11, 1997 [1, 2].

As a result of the vigorous industrial activities of the industrialized nations, the UNFCCC placed onus on them for higher levels of GHG emissions in the atmosphere and thus came heavily on the developed nations under the principle of “common but differentiated responsibilities”. The Kyoto Protocol legally commits its Parties by setting internationally binding emission reduction targets. The detailed rules for the implementation of the Kyoto Protocol were adopted at COP 7 in Marrakesh, Morocco, in 2001, and are referred to as the "Marrakesh Accords". The Kyoto Protocol came into force on February 16, 2005 and targets six main green house gases: Carbon Dioxide (CO2); Methane (CH4); Nitrous Oxide (N2O); Hydro Fluorocarbons (HFCs); Per Fluorocarbons (PFCs); and Sulphur Hexafluoride (SF6). The six GHG are translated into CO2 equivalents in determining reductions in emissions [1, 2, 3].

As per the Kyoto Protocol, the industrialized nations (referred to as Annex I countries [1, 2] which includes Australia, Austria, Belarus, Belgium, Bulgaria, Canada, Croatia, Cyprus, Czech Republic, Denmark, Estonia, European Union, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Japan, Latvia, Liechtenstein, Lithuania, Luxembourg, Malta, Monaco, Netherlands, New Zealand, Norway, Poland, Portugal, Romania, Russian Federation, Slovakia, Slovenia, Spain, Sweden, Switzerland, Turkey, Ukraine, United Kingdom of Great Britain, Northern Ireland and USA) ratifying the protocol are bound to reduce green house gas emissions by an average of 5 % below 1990 levels (base year for most of the parties to Kyoto Protocol) by the first commitment period of 2008 to 2012. These reduction targets are in addition to the industrial gases, chlorofluorocarbons, or CFCs, which are dealt with under the Montreal Protocol (1987) on Substances that Deplete the Ozone Layer [2, 3].

An amendment to the Kyoto Protocol was adopted on December 08, 2012 at a UN Climate Change Conference held at Doha, Qatar. This amendment to the Kyoto Protocol is referred to as “Doha Amendment to the Kyoto Protocol". The salient features [2] of this amendment are:

(a) A next commitment period of eight years for GHG emissions reduction was targeted from January 01, 2013 to December 31, 2020.

(b) A revision of the commitments along with a revised list of GHG to be reduced and reported by the Annex I countries who agreed to carry forward in the next commitment period of Kyoto Protocol.

(c) A minimum target of 18% reduction below 1990 levels in GHG emissions is to be achieved within the time span of eight years of the second commitment period.

(d) The composition of Parties in the second commitment period is different from the first commitment period.

As per the Kyoto Protocol, the signatories to the Kyoto Protocol have to meet their GHG reduction targets primarily through targeting their national means and measures. But, the Kyoto Protocol also provides some flexibility to these countries by providing three international market-based mechanisms to achieve their reduction targets. These mechanisms are International Emissions Trading, Clean Development Mechanism (CDM) and Joint implementation (JI). A brief description [1, 2] of the mechanisms of Emission Trading and Joint Implementation (CDM is discussed in detail in the next section) is as follows:

Parties with commitments under the Kyoto Protocol (Annex B Parties which is nearly identical list as Annex I except Belarus or Turkey [4]) have accepted targets for limiting or reducing emissions. These targets are expressed as levels of allowed emissions, or "assigned amounts". The allowed emissions are divided into "assigned amount units" (AAUs). Emissions trading, as set out in Article 17 of the Kyoto Protocol, allows countries that have emission units to spare - emissions permitted them but not "used" - to sell this excess capacity to countries that are over their targets. Thus, a new commodity was created in the form of emission reductions or removals. Since carbon dioxide is the principal greenhouse gas, people speak simply of trading in carbon. Carbon is now tracked and traded like any other commodity. This is known as the "carbon market."

The mechanism known as "joint implementation" defined in Article 6 of the Kyoto Protocol, allows a country with an emission reduction or limitation commitment under the Kyoto Protocol (Annex B Party) to earn emission reduction units (ERUs) from an emission-reduction or emission removal project in another Annex B Party, each equivalent to one tonne of CO2, which can be counted towards meeting its Kyoto target.

2. CLEAN DEVELOPMENT MECHANISM (CDM): AN INTRODUCTION

Although the Annex I countries are supposed to meet their GHG reduction targets primarily on their own but this flexibility mechanism of CDM under Article 12 of the Kyoto Protocol is provided with the dual intention of sustainable development of developing countries in a comparatively easy, flexible and cost effective way by the Annex B countries (industrialized countries) while attaining their reduction targets through clean and green projects in developing countries. For example; it requires US $50 for mitigating one ton of CO2 equivalent in developed countries whilst in developing countries the same can be done at the rate of US $15 per ton of CO2 equivalent. While investors profit from CDM projects by obtaining reductions at costs lower than in their own countries, the gains to the developing country host parties are in the form of finance, technology, and sustainable development benefits. Out of three mechanisms of Kyoto Protocol, CDM is the only mechanism where developing countries can

participate in the Protocol and join the global offers to mitigate the climate change. CDM is the first global, environmental investment and credit scheme of its kind, providing a standardized emission offset instrument, known as Certified Emission Reduction (CER) credits [5].

CDM grants Annex B countries the right to generate or purchase some Certified Emission Reduction (CER) credits, each equivalent to one tonne of CO2, from projects undertaken outside Annex I countries i.e. in the countries which do not have binding emission reduction targets, since greenhouse gases have the same impact no matter where they are emitted they should be reduced where it is less costly and feasible. Thus, provides industrialized countries some flexibility in how they meet their emission reduction or limitation targets [2, 5].

A CDM project must be able to avoid emissions that would otherwise have occurred. Some typical CDM projects may be Power Generation through renewable resources, Installation of solar lights or solar heaters, Installation of more energy efficient air-conditioning systems or heating systems or industrial boilers, etc.

3. GOVERNANCE MECHANISM OF CDM

The Governance of CDM is made through CDM Executive Board, Panels and Teams, National Authorities, Validators and Verifiers.

The CDM Executive Board (CDM EB) supervises the Kyoto Protocol's clean development mechanism under the authority and guidance of the Conference of the Parties serving as the Meeting of the Parties to the Kyoto Protocol (CMP). The CDM EB is fully accountable to the CMP. The CDM EB will be the ultimate point of contact for CDM Project Participants for the registration of projects and the issuance of CERs. The CDM Executive Board (CDM EB) may establish committees, panels or working groups to assist it in the performance of its functions. The CDM EB shall draw on the expertise necessary to perform its functions, including from the UNFCCC roster of experts. In this context, it shall take fully into account the consideration of regional balance [5, 6].

The various established teams or panels or working groups under CDM EB are [5, 6]: Methodologies Panel (Meth Panel); Afforestation & Reforestation Working Group (A/R WG); Small Scale Working Group (SSC WG); Accreditation Panel (CDM AP); Registration and Issuance Team (RIT); Carbon Dioxide Capture and Storage Working group (CCS WG).

The Meth Panel, A/R WG SSC WG, CCS WG were established to prepare recommendations to CDM EB on submitted proposals for new baseline and monitoring methodologies in their respective fields and maintain close liaison amongst themselves.

The Accreditation Panel was established to develop recommendations and facilitate the decision making of the CDM EB in accordance with the standards and procedure for accrediting operational entities. A designated operational entity (DOE) (act as Validator and Verifier on behalf of CDM EB) is an independent auditor accredited by the CDM Executive Board (CDM EB) to validate project proposals or verify whether implemented projects have achieved planned greenhouse gas emission reductions.

The CDM Registration and Issuance Team is a group of external experts that assist the CDM EB by assessing requests for registration of project activities or programmes of activities as well as requests for issuance for which review has been requested.

A designated national authority (DNA) is the organization granted responsibility by a Party or host country to authorise and approve participation in CDM projects. Establishment of a DNA is a primary requirement for participation by a Party in the CDM. The primary task of the DNA is to evaluate potential CDM projects for their suitability to the host country in achieving its sustainable development goals, and upon satisfaction to provide a letter of approval to project participants in CDM projects. This letter of approval must declare that the project activity contributes to sustainable development in the country, that the country has ratified the Kyoto Protocol, and that participation in CDM is voluntary and no hidden motives. It is then submitted to CDM Executive Board to support the registration of the project. DNAs have additional roles to play, such as the submission of proposed standardized baselines for their country, among others. These responsibilities have increased as the CDM has evolved [5, 6].

The following Figure 1 (Source: [5]) depicts the Cycle of Project Development under CDM. This cycle also depicts the role of governing bodies of CDM in various project development stages:

Figure 1 (Source: [5]): Cycle of Project Development under CDM

4. CDM PROJECTS: AN OVERVIEW

Table 1 (source [7]) depicts the technology types that are being transferred from which country to which country as a result of CDM projects. Table 2 depicts the host countries of CDM projects along with their number of CDM projects bagged and also their percentage share in the total registered projects. This table shows only those host countries which have more than one percent share in the total registered CDM projects. Table 3 classifies the CDM projects by the regions recognized by the UNFCCC as well as enumerates the absolute and respective percentage share of these regions in the total registered CDM projects. Table 4 classifies the CDM projects based on their size i.e. small and large. Table 5 depicts the classification of CDM projects by Scope i.e. the major sector of their operations. Table 6 depicts the CERs issued by each of the host countries of CDM projects and their percentage share in the total CERs issued. This table also recognizes only those host countries which have more than one percent share in the total CERs issued. Table 7 provides the cumulative and Year-wise break-up from 2004 to 2018 of total registered CDM projects in top 10 countries i.e. those countries having greater than 1% share of total registered projects and also of all other countries involved in CDM projects. Table 8 classifies the methodologies or tools or techniques approved by the CDM EB for use in the GHG reduction on the basis of scope sector. This table also classifies these approved methodologies on the basis of their applicability i.e. in small scale projects or large scale projects or both (consolidated).

Type of technology	Main countries of origin	Main countries of destination
Biomass energy	Belgium, Denmark, Japan	Malaysia, India, Brazil, Indonesia
Wind power	Denmark, Germany, Spain, USA	China, India, Brazil, Mexico
Landfill gas	Italy, UK, France, USA, Ireland, Netherlands	Brazil, Mexico, Argentina, Chile, China
HFC decomposition	France, Germany, Japan	China, India
Hydro-power	France, Germany, UK, Spain	Ecuador, Panama, Honduras, South Korea, Mongolia
Agriculture	Ireland, Canada, UK	Mexico, Brazil, Philippines, Ecuador
Energy efficiency in industry	Japan, Italy, USA	India, China, Malaysia
N2O destruction	Germany, Japan, France	South Korea

Table 1: Beneficiary Countries of Technology Transfer due to CDM Projects [7]

Host Party	Number Of Projects	Percent
China	3764	48.23
India	1667	21.36
Brazil	343	4.39
Viet Nam	255	3.27
Mexico	192	2.46
Indonesia	147	1.88
Thailand	144	1.84
Malaysia	143	1.83
Chile	103	1.32
Republic of Korea	88	1.13

Table 2: Distribution of registered projects by Host Party (only those with >1% share) (from 2004 to 2018) [8]

Region	No. of Projects	Percent
Africa	218	2.79
Asia & Pacific	6533	83.71
Economies in Transition	49	0.63
Latin America & Caribbean	1004	12.86

Table 3: Distribution of registered projects by UNFCCC region (from 2004 to 2018) [8]

Scale	No. of Projects	Percent
Large	4676	59.92
Small	3128	40.08

Table 4: Distribution of registered projects by Scale (from 2004 to 2018) [8]

Scope No.	Scope Label	No. of Projects	Percentage
1	[1] Energy ind. (ren/non-ren)	6526	75.2
13	[13] Waste handling and disposal	931	10.73
4	[4] Manufacturing ind.	376	4.33
15	[15] Agriculture	202	2.33
10	[10] Fugitive emiss. (solid/oil/gas)	163	1.88
3	[3] Energy demand	136	1.57
5	[5] Chemical ind.	118	1.36
8	[8] Mining/mineral prod.	84	0.97
14	[14] Afforestation/reforestation	66	0.76
7	[7] Transport	30	0.34
11	[11] Fugitive emiss. (halon/SF6)	25	0.29
9	[9] Metal production	13	0.15
2	[2] Energy distr.	8	0.09

Table 5: Distribution* of registered projects by Scope (*Note that a project may be considered in more than one scope sector) (from 2004 to 2018) [8]

Host Party	No. of CERs	Percent
Brazil	1.44E+08	7.31
Chile	29953561	1.52
China	1.09E+09	55.3
India	2.47E+08	12.6
Indonesia	32614450	1.66
Mexico	33190293	1.69
Republic of Korea	1.78E+08	9.04
Vietnam	22250742	1.13

Table 6: Percentage CERs issued from registered projects in a Host Party (having more than 1% share) (from 2005 to February 2019) [8]

	No. of Registered Projects in														
Host Party	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018
Cumulative of Top 10 Countries (Having > 1% share)	1	35	344	368	381	600	750	991	2898	241	110	73	28	26	7
Total (Cumulative of All Countries Involved)	1	62	409	425	431	684	809	1107	3235	297	158	91	52	39	11

Table 7: Year-wise break-up of total registered CDM projects in top 10 countries and all countries involved [8]

Scope	No. Of Method-ologies (All)	Perc-entage (All)	Small Scale	Perc-entage (small scale)	Large Scale	Perc-entage (Large scale)	Cons-olidate d	Perc-entage (conso-lidated)
[1] Energy Industry (renewable/non-renewable)	71	27.2	20	18.52	35	29.91	16	44.44
[2] Energy Distribution	9	3.45	6	5.55	3	2.56	0	
[3] Energy Demand	31	11.88	19	17.6	12	10.25	0	
[4] Manufacturing Industry	34	13.03	13	12.04	15	12.82	6	16.67
[5] Chemical Industry	23	8.81	7	6.48	14	11.96	2	5.55
[6] Construction	1	0.38	1	0.92	0		0	
[7] Transport	20	7.66	13	12.04	5	4.27	2	5.55
[8] Mining/Mineral Production	1	0.38	0		0		1	2.78
[9] Metal Production	9	3.45	0		9	7.69	0	
[10] Fugitive Emissions (solid/oil/gas)	9	3.45	2	1.85	6	5.13	1	2.78
[11] Fugitive Emissions halon/SF6)	10	3.83	2	1.85	8	6.84	0	
[13] Waste Handling and Disposal	27	10.34	15	13.89	7	5.98	5	13.89
[14] Afforestation/ Reforestation	4	1.53	2	1.85	1	0.85	1	2.78
[15] Agriculture	12	4.6	8	7.41	2	1.71	2	5.55

Table 8: Approved methodologies by scope (Note that a methodology can be linked to more than one sectoral scope as well as scale of the project) [8]

5. DISCUSSION AND CONCLUSION

Globally, the maximum number of technology transfer (including equipment) took place in the sector of Bio-mass Energy and Hydro-Power Projects although the percentage of these projects in which technology transfer took place is low due to the fact a large number of CDM projects were registered in these fields. India is also a beneficiary of technology transfer but share is quite less in comparison to countries like Brazil, China and Mexico [7].

China leads in terms of number of CDM projects bagged and India is the next but the margin in between is quite large. The major share of the CDM projects lies in the Asia Pacific region.

China also tops the list of share of CERs issued from these CDM projects and India is next but again the margin in between is quite high. Thus, it can be said that China is deriving the most and far ahead in obtaining the quantitative as well as qualitative benefits from these CDM projects [8].

Globally the CDM projects are mainly in the field of Energy Industries with a heavy presence in the field of renewable energy. This may also be due to the fact the largest number of approved methodologies for GHG mitigation are in this field only. Waste Handling and disposal, and manufacturing sector are the next two scope sectors but with a large gap. This necessitates the introduction, exploration and innovation of more and more methodologies in diverse fields or scope sectors, especially the manufacturing and process industries sector, for GHG reduction or mitigation [8].

The majority share of CDM projects are in the scope sector of Wind Energy and Hydro Power. This global pattern is also true for India [8, 9]. In India, Karnataka, Maharashtra and Tamil Nadu are the favourite destinations of these CDM projects and mainly the projects are in the field of renewable energy [10].

Although the statistics portrays a satisfactory situation, a larger investigation is required in regard to the actual sustainable development of the host countries of these CDM projects. The number of registered CDM projects spiked in the year of 2012 which needs an analysis to capture the favourable circumstances. Moreover, the technical difficulties and costs associated with the CERs as well as project registrations [11] also warrant a thorough investigation.

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